THE KLYSTRON RF SYSTEMS FOR THE INDIANA UNIVERSITY LENS ACCELERATOR*

William A. Reass and Daniel E. Rees,
Los Alamos National Laboratory, Los Alamos, NM 87545, U.S.A.

Vladimir P. Derenchuk, Thomas C. Rinckel, and Gerard J. Visser,
Indiana University, Bloomington, Indiana, U.S.A.

Abstract

This paper describes the Klystron RF systems for the Indiana University Low Energy Neutron Source (LENS) accelerator 425 MHz Radio Frequency Quadrupole (RFQ) and Drift Tube Linac (DTL) systems. Of interest in the power conditioning system is the design of the totem-pole grid-catch modulator for the mod-anode klystrons. This topology provides a fast rise and fall and closed loop regulation for the klystron mod-anode to cathode voltage, which minimizes RF amplitude and phase droop while maximizing efficiency. Another advantage is that short pulse high rep-rate operation is viable within the average power capabilities of the klystron. The 425 MHz, 1.25 MW klystron amplifier chain will also be detailed. Of final interest, is the digital low level RF system. This provides vector control of the cavity field using direct conversion, non-I/Q sampling architecture, at a sampling rate of 132 MHz with a 12-bit analog-to-digital converter (ADC). Four input and two output channels are integrated into a 6 unit (6U) VME module, with all DSP functions performed in Xilinx Spartan-3 field-programmable gate arrays. The design and implementation of these systems, coupled with LENS operational results, will be presented.

Low Level RF Controls

Modern low level RF control systems often involve digital techniques [1], [2]. We make no attempt to buck that trend. The LENS [3] low-level RF control system is a highly integrated design utilizing wideband pipelined converters and digital signal processing.

The 425 MHz cavity signal sample is directly digitized by a Linear Technologies LTC2220 12 bit ADC. The signal is undersampled, using a reference clock (ADC sample clock) frequency of 132 MHz. In particular it should be noted that this is a non-I/Q sampling scheme [4], and it does not rely on any particular relationship between the operating and reference frequencies. Digital signal processing is performed in a Xilinx "Spartan-3" FPGA. The 29 MHz digital input signal is multiplied by a complex 29 MHz reference generated by a CORDIC algorithm and then low pass filtered with a 19-tap symmetric FIR filter (-3dB bandwidth 3.5 MHz) to extract the measured cavity field vector. The total delay from the analog RF input to the FIR filter output is 18 cycles, that is 136 ns. A brute force approach is taken to reduce roundoff error – since the FPGA multiplier blocks are 18 bit, the entire digital signal path uses 18 bit arithmetic.

The measured cavity field is subtracted from the setpoint vector and fed into a proportional-integral controller with a saturating integral term. The controller output is added to a feedforward vector to produce the output drive control vector. All the parameters (complex setpoint, real proportional and integral gains, and complex feedforward value) are taken from a piecewise constant waveform table, allowing up to 1024 values with programmable dwell. Only simple, manually programmed control waveforms have been used to date, but we have designed this with a view to use adaptive feedforward control in the future. For diagnostics, as well as for adaptive feedforward, the raw ADC signal, the measured complex cavity signal, and the complex drive signal are all captured (simultaneously) in "oscilloscope" buffers. Up to 2048 points are stored at the full clock rate or with a selectable decimation. The control waveform tables and the oscilloscope buffers are all implemented in 34 kBytes of the FPGA's dual-port memory blocks.

The error signal into the controller is continuously checked against programmable bounds, and if it exceeds them the RF drive is killed for the remainder of the pulse.

The drive control vector digitally modulates (through a complex multiplier) an independent 29 MHz complex reference from another CORDIC block. The reference phase is set to compensate the overall loop phase so that the controller gains can be taken as positive real numbers. The complex digital output goes to a dual 14-bit DAC, which drives a quadrature modulator to produce the RF output. An on-board PLL frequency multiplier produces the required 396 MHz reference. The RF output is buffered and amplified (typical output +14 dBm). Overall control loop delay must be minimized for optimal control; we achieve 960 ns, observable on the controller's response to a feedforward step.

The complete LLRF channel fits into an 86 by 50 mm printed circuit board area. A picture is shown in Figure. The FPGA design utilizes merely 29% of the available logic resources, although nearly all of the multiplier blocks. Four LLRF channels are integrated on a 6U x 160 mm VME board, with the reference multiplier PLL,

* Work supported by the National Science Foundation (grants DMR-0220560, DMR-0320627), the 21st Century Science and Technology fund of Indiana, Indiana University, and the Department of Defense.

VME interface, opto-isolated interlock inputs and outputs, and power supplies. A (750 kHz) switching converter is required in order to power the 1.2 V FPGA's with reasonable efficiency from the 5 V bus. No interference from this is discernable in the signal path.

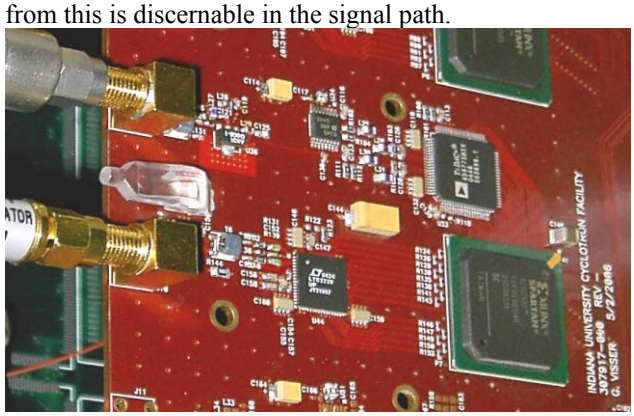

Figure 1: The complete LLRF channel: RF in (lower connector), digital signal processing, RF out (upper connector).

In the present LENS system, two LLRF channels are actually used for control, and six further channels simply monitor forward and reflected power at various points, that can also provide protection trip functions. The LLRF boards are controlled through the VME bus and a shared memory interface to the controls computer, a DEC Alpha workstation running Vsystem [5] from Vista Control Systems, Inc. Besides setting parameters, the controls software reads and display any two selected LLRF oscilloscope buffers in real time at over 20 Hz pulse rate.

Figure illustrates the DTL klystron drive output of the low level RF system in operation with a 100 µs beam pulse at roughly 15 mA, on a 179 µs RF pulse. In the first 29 µs of the pulse, the feedforward drive alone is used to ramp up the cavity to near the setpoint; only then the proportional and integral gain terms are turned on and the controller makes the required small correction, holding the cavity amplitude within ±1.2 % and phase within ±0.5 ° including during the beam turn-on and turn-off transients. Feedback gain was not yet carefully optimized during this operation.

For longer pulse operation (>1 ms), since the low level RF system must cancel the rather large klystron phase shift droop (37 degrees/ms) due to the cathode supply voltage droop during the pulse, the stability of the control loop would be compromised. To compensate this, the reference frequency of the digital modulator will be offset by +103 Hz so the control loop only sees a small residual phase deviation and control loop stability is maintained.

Klystron Modulator System

The IUCF LENS accelerator klystron RF power systems are based on the developments, designs, and surplus equipment from the Los Alamos Ground Test Accelerator (GTA), Strategic Defense Initiative (SDI) program [6]. Many LENS operational parameters are very similar to the GTA requirements as related to frequency, pulse width, and peak RF power. The use of

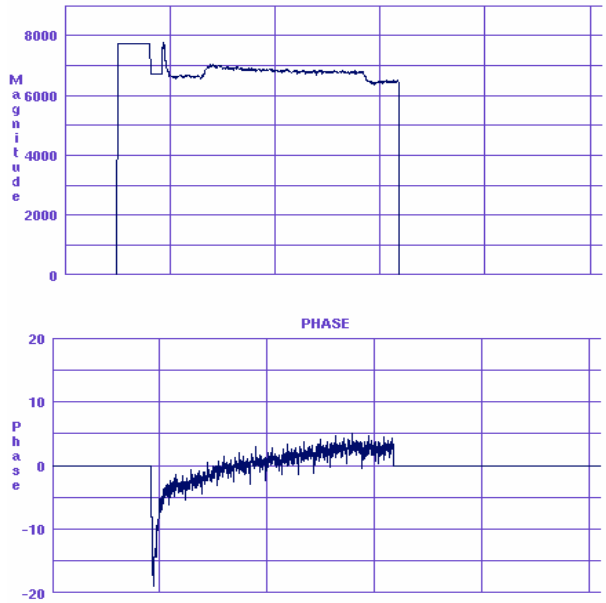

Figure 2: RF drive vector control for the DTL, measured by LLRF board "oscilloscope" buffer and displayed on the operator's screen. Horizontal axis is 68 µs/div.

this equipment provides significant savings as compared to a purchase of new equipment, although modern high-efficiency klystron designs are now available. To improve the modulator switching performance a "tail-biter" planar triode tube will be added to the GTA designed grid-catch modulator.

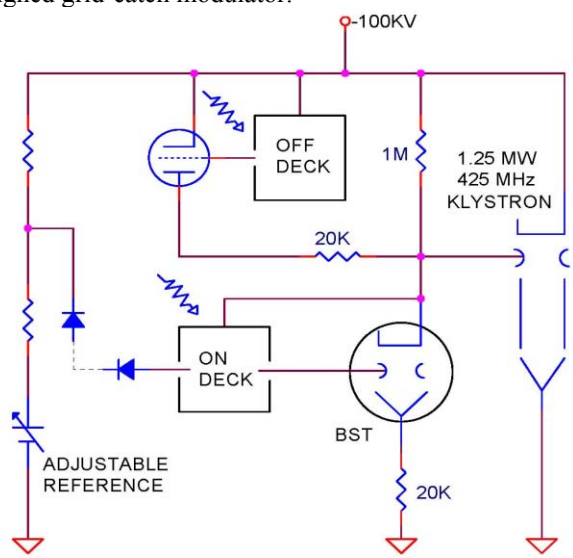

Figure 3: Klystron grid-catch modulator with tail biter.

The grid-catch modulator, as shown in Figure 3, uses a magnetron injection gun hollow beam switch tube (BST) in a cathode follower circuit to regulate the klystron mod-anode voltage. This tube is driven by the fiber-optic controlled "on-deck" and clamps at the voltage determined by the reference voltage divider, when the isolation diodes become forward biased during the switching cycle. By increasing the BST mod-anode voltage drive, as compared to the GTA design, improved

turn-on time results. To improve the fall time, a H.V. planar triode tube is used to discharge the klystron mod-anode (and deck) capacitance. The tail-biter triode is controlled via fiber optic signals to the "off-deck". A fiber-optic repeater in the modulator oil tank derives the control signals for the on and off decks such that "shoot-through" events do not occur.

Klystron HV Power System

The high-voltage capacitor bank system is somewhat unique (Figure 4) in that 2 uF, 100kV plastic cased capacitors are utilized. The design of the plastic case provides the insulation between the –HV and ground terminals. The capacitors are on a common buss with individual fault current limiting resistors. A conventional (GTA) spark-gap crowbar system is used to divert fault energy from the klystron when arc-down events occur. A crowbar test wire ensures fault energy is less than 10 Joules.

Figure 4: HV capacitor bank with plastic capacitors.

Klystron Control and Monitor System

To complete the klystron RF system, the IUCF low level RF controls were added to the 90's vintage GTA transmitter racks as shown in Figure 5. These contain all the typical sub-systems such as klystron RF and HV fault protection logic, klystron filament and solenoid supplies, vac-ion pumps, HV power supply and cap room controls, PLC controls, as well as the RF amplifier chain.

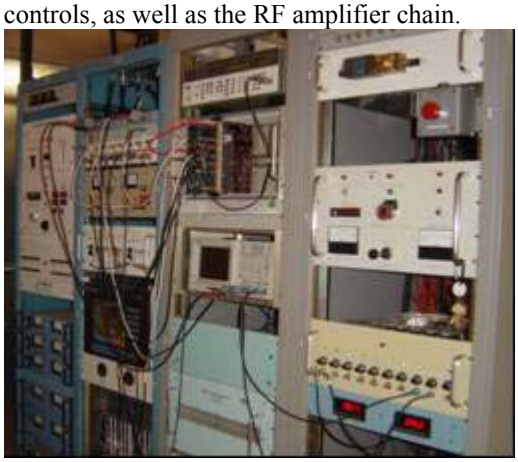

Figure 5: LENS klystron RF transmitter racks.

Klystrons and Modulator Tank

A view of the klystrons fitted to the GTA modulator tank is provided in Figure 6. The overall height is about 12 feet and the output waveguide is WR2100.

Figure 6: LENS klystrons and modulator tank.

CONCLUSION

The overall operation and testing is going very smoothly and additional GTA style hardware, klystrons, and advanced IUCF designed LLRF controls will be utilized for the final 13 MeV configuration. The final DTL tank will be received in September and additional power conditioning, RF driveline, and waveguide runs are being designed to accommodate the Indiana University LENS accelerator operational schedules.

REFERENCES

[1] M. Champion et al, "Overview of the Spallation Neutron Source Linac Low-Level RF Control System", PAC 2005, Knoxville, Tennessee.

[2] S.N. Simrock, "State of the Art in RF Control", LINAC 2004, Lübeck, Germany.

[3] A. Bogdanov et al., "Upgrade of the LENS Proton Linac: Commissioning and Results", PAC 2007, Albuquerque, New Mexico

[4] L. R. Doolittle et al, "Digital Low-level RF Control Using Non-I/Q Sampling", LINAC 2006, Knoxville, Tennessee.

[5] P.N. Clout et al, "A Comparison of Vsystem and EPICS", ICALEPCS'97, Beijing, China (1997).

[6] W. North and W. Reass, "Electrical Design of a Two-Klystron RF Station for the Los Alamos National Laboratory Neutral Particle Beam Experiment", 1992 Modulator Symposium, Myrtle Beach, S.C. pp15-18.

