DESIGN AND MEASUREMENTS OF A DAMPING RING KICKER FOR THE ILC

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Abstract

The International Linear Collider (ILC) requires ultra fast kickers for the damping ring. The modulators must produce pulses of ±5 kV magnitude, with rise and fall times of 6 ns or less depending on the final configuration [1]. The deflector plates will be configured as a 50 Ω stripline, charged to opposite polarities, providing a potential difference of 10 kV. The pulse magnitude must be repeatable to a high accuracy. The need for 3.25 MHz burst mode operation, at 5 Hz, gives an average repetition rate of up to 16.3 kHz [2]. This paper describes a novel design for a pulse generator for the damping ring kickers, in which two stacks of 1 kV FETS will be combined to generate the fast pulses. Each stack of FETs is a 100 Ω driver: the two stacks form a 50 Ω pulse generator as this is preferable to one 50 Ω stack. Measurements and calculations are presented on the present state of the TRIUMF prototype pulse generator.

INTRODUCTION

The 2005 ILC damping ring baseline considered a damping ring with bunch spacing in the range 3 ns to 14 ns [1]. However a recent baseline suggests a pulse width of ≤4.16 ns, with a burst mode of 3.25 MHz, and voltage fluctuations of individual kickers of ≤0.33% [2].

The injection/extraction kickers have to provide 0.6 mrad deflection of 5 GeV bunches. The beam bunches will travel in the opposite direction to the stripline pulse and thus the total deflection (θ) will be the sum of the magnetic (θ_B) and electric (θ_E) components of the deflection. The total deflection is given by:

$$\theta = \theta_B + \theta_E = \frac{0.3 \cdot V \cdot l_s}{d \cdot p \cdot c}\left(1 + 1/\beta\right) \qquad (1)$$

where V is the potential difference between the stripline plates, l_s is the overall length of stripline plates, d is the plate separation, $\beta \cdot c$ is particle velocity, c is the velocity of light in free space (3×10^8 m/s), and p is the beam momentum in units of GeV/c. In this case $\beta = 1$ so that the electric and magnetic deflections are equal.

To allow for adequate rise-time of the electrical pulse, sets of striplines mechanically in series are required. To minimize the effective field rise-time, the sets of striplines must be energized at the appropriate time [3]. The permissible pulse rise-time (t_p) is given approximately by:

$$t_p = t_b - 2 \cdot l_s / (N \cdot c) \qquad (2)$$

where, (t_b) is the beam gap and N is the number of sections into which the total stripline length is sub-divided. If the beam gap is 6 ns and each set of striplines is 30 cm long (l_s/N), i.e. 1 ns fill time, t_p=4 ns. To achieve 0.6 mrad deflection, approximately 20 such kickers are needed with the plates pulsed to ±5 kV.

DRIVER CONCEPTS

The TRIUMF kicker group has developed a new circuit concept for a prototype damping ring kicker for ILC. The design of the ILC modulator is based on previous designs at TRIUMF (Table 1) but with significant modifications. All of these previous designs employed 2 stacks of 1 kV FET modules operating in push-pull mode. The MuLan kicker design [4, 5] permits operation from DC up to more than 75 kHz continuous at voltages of up to ±12.5 kV into a capacitive load. The RFQ pulser [6] for TITAN has been tested at 600 V peak-peak at 2.2 MHz, and 500 V peak-peak at 3.0 MHz continuous operation.

Proof of principal tests for the ILC damping ring kickers were performed using the MULAN prototype kicker as a test bed and components on hand, including DE375-102N12A FETs and DEIC420A FET drivers. A 3.1 Ω resistance, previously connected between the driver output and FET gate [4], was reduced to 0.5 Ω to increase transient gate-current. Pulses of 4.6 kV, with 6 ns rise and fall times (10% to 90%) and 21 ns width (at the 5% level), were generated across a 100 Ω load at 1 kHz. Subsequently the FET modules, the backplane which the modules plug into, and the mounting stand were re-designed: a module and its backplane connection is termed a level. The goal of the redesign was to reduce pulse width by decreasing inductance and capacitance of each level while maintaining adequate airflow for cooling.

Table 1. Measured values for TRIUMF MOSFET kickers

Pulse voltage	Rise and fall time	Repetition rate (continuous)	References
6 kV	30 ns	10 Hz to 20 kHz	See [4]
10 kV	40 ns	10 Hz to 1 MHz	See [4]
±10 kV	100 µs	<10 mHz to 10 Hz	See [4]
−3.5 kV	63 ns	DC to 52.2 kHz	See [4]
±12.5 kV	40 ns	DC to 77 kHz	[4]
500V	120 ns	3 MHz	[6]

ILC Pulser Concept

As a result of the relatively low impedance of the damping ring kickers, the proposed design does not require push-pull operation of stacks to achieve fast rise and fall times. The prototype ILC kicker consists of a stack of 15 series, 1 kV, modules configured to form a delay line. Each level has a capacitance to ground (C) that is almost independent of its position in the stack, with the exception of the end modules which have an additional ~1 pF to ground. The characteristic impedance (Z) of each level of the stack is given by Eq. 3, where L is the series

Now employed at CERN, Switzerland.

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inductance of a level of the stack.

$$Z = \sqrt{L/C} \quad (3)$$

The propagation time of a pulse through each level (τ) is given by

$$\tau = \sqrt{L \cdot C} \quad (4)$$

The rise and fall time of the pulse generated is related to the intrinsic switching time of each FET, the number of series FETs (15) and the pulse propagation time through each level of the delay line. The number of series FETs is dependent upon the voltage rating of each FET and the required voltage rating of the stack: FETs with a switching time of 2 ns to 3 ns [5] are available up to 1 kV. To achieve a fast rising/falling pulse it is necessary to minimize propagation delay and hence inductance. The DEI FETs used have a low inductance, hence the stack inductance is mainly dependent upon the backplane connection between FETs. Eq. 3 and Eq. 4 show that, for a given minimum inductance, the delay of a 100 Ω line is less than that of a 50 Ω line and hence the stack was configured to have an impedance of ~100 Ω.

The deflection is independent of the impedance of the striplines and the deflections due to the electric and magnetic fields are equal for $\beta=1$ (Eq. 1). To make use of commercially available components, such as coaxial cable and feed-throughs, it is preferable to select a system impedance of 50 Ω: a driver impedance of 50 Ω can be achieved with 2 parallel 100 Ω stacks.

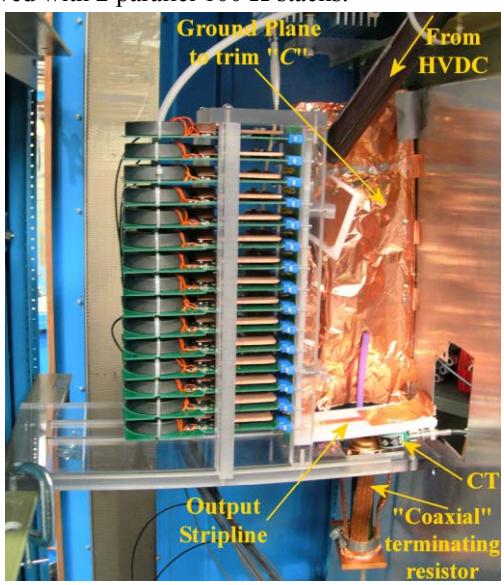

Figure 1: Stack of 15 series FETs configured as a 100 Ω delay line (no heat sinks mounted on cards).

The FET stack (Fig. 1) is charged, from a DC supply, through a 10 kΩ resistor connected to the drain of the top FET. The source of the bottom FET is connected to a "coaxial" 104 Ω terminating resistor. The stack is charged and subsequently the 15 FETs are turned on, within 0.7 ns of each other, to discharge the energy stored in the capacitance of the stack into the terminating resistor. The FET stack is turned off ~160 ns later when there is negligible current flow and the stack is then recharged. The minimum on-time of 160 ns is a limitation of the present fiber optics, used to trigger the FETs, and will be addressed for 3.25 MHz burst mode operation.

Measurement of Driver Parameters

Measurements were made on the prototype stack to determine the value of parameters τ, L, C and Z. The value of τ was determined by measuring the propagation delay through the 15 series levels. The FETs were all held in the on-state and an 8 V pulse was fed through a 50 Ω coax to the drain of the top FET. Given that the impedance of the stack was close to 100 Ω, another 100 Ω resistor was placed in parallel with the stack to provide a reasonable match to the 50 Ω source impedance of the pulse generator. The measured propagation time through 15 levels was 3.1 ns, which corresponds to 0.21 ns/level.

The inductance of the stack ($15 \cdot L$) is given by;

$$15 \cdot L = \frac{1}{I}\int\left(V_{in} - V_{out[in]}\right) \cdot dt \quad (5)$$

where I is the load current, V_{in} is the input voltage to the stack, and $V_{out[in]}$ is the output voltage of the stack normalized to the input voltage. Normalization of the output voltage accounts for the on-state resistance of the FETs. The resultant inductance of the stack is 450 nH±25 nH, which corresponds to 30 nH±1.7 nH per level. The spacing between modules on the backplane (Fig. 2) is 20 mm which accounts for ~20 nH and the remaining 10 nH is due to the FET and the power traces on the module.

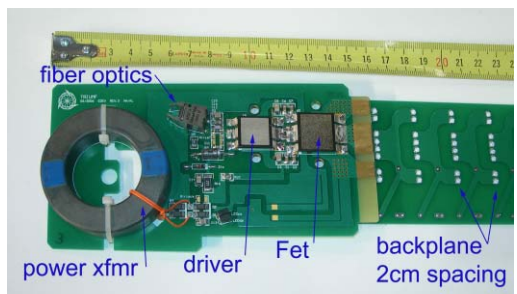

Figure 2: Low inductance FET module and backplane.

The stack capacitance was determined by charging it through a 5.32 kΩ resistor and measuring the RC time constant: the FETs were in the on-state and the output of the stack was open-circuit. The average, of 1.75 pF/level, is in good agreement with the theoretical value [5].

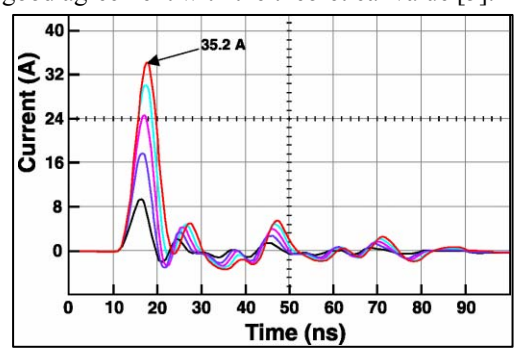

Figure 3: Pulse for 2.5kV, 5kV, 7.5kV, 10kV, and 12.5kV DC supply; C=1.75 pF (before increasing capacitance).

L=30 nH & C=1.75 pF corresponds to Z=130 Ω and

τ=0.23 ns/level: this delay is consistent with the direct measurement of 0.21 ns/level. Fig. 3 shows measured HV pulses: the post-pulse reflections are due to impedance mismatches. Charging the FET stack to 12.5 kV gives 35.2 A peak (measured using a Pearson 2877 CT with a specified useable rise-time of 2 ns and a 500 MHz Tektronix TDS 7104 oscilloscope) into a 104 Ω load. This corresponds to a peak load voltage of 3.66 kV. The amplitude is lower than 12.5 kV/2 because the stack impedance is high, the FETs have an on-state resistance of ~1 Ω each and the parasitic capacitances to ground of each level in the delay line are not all pre-charged to 12.5 kV due to (resistive) voltage grading down the stack.

To decrease Z, C was increased: this was achieved by installing an additional ground plane beside the stack (Fig. 1). By trial and error the magnitude of the post pulse reflections were reduced, which is an indication that the characteristic impedance is matched to the terminator. Re-measuring gave an average C of 3.3 pF/level. Fig. 4 shows the measured HV pulses for C=3.3 pF with 15 pF added to the drain of the top FET: the pulse magnitude, rise-time and width are increased in comparison with Z=130 Ω (Fig. 3). The output current magnitude is 46.2 A (4.8 kV into 104 Ω) for 12.5 kV DC. The measured 10% to 90% rise-time is 4.3 ns. Assuming that neither the CT nor oscilloscope causes overshoot of the pulse, the actual rise-time of the current can be estimated to be 3.7 ns [3]. A higher bandwidth measurement system is required to more accurately determine the rise-time of load current.

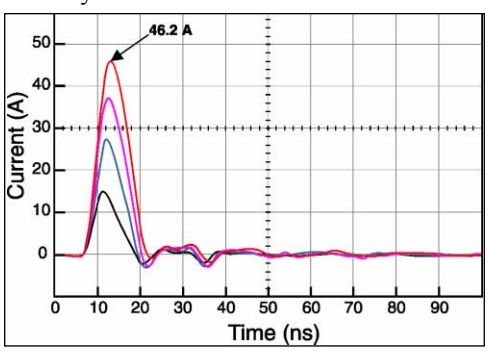

Figure 4: Pulse for 3 kV, 6 kV, 9 kV & 12.5kV DC, for C=3.3 pF & with 15 pF added to the drain of the top FET.

In Figs. 3 and 4 the amplitude of the pulse does not increase linearly with the applied DC voltage, however the area of the pulse is proportional to the charge stored on the stack. PSpice also demonstrates the same effect, which is attributable to Miller capacitance of the FETs: increasing the gate drive, in the PSpice simulation, reduces the non-linearity. In Fig. 3 the full pulse width varies from 7.7 ns for 2.5 kV DC to 10.6 ns for 12.5kV DC, whereas in Fig. 4 the full pulse width varies from 11.5 ns for 3 kV DC to 13.7 ns for 12.5kV DC.

The FETS in the stack were deliberately positioned in the order of the measured delay of each FET, with the top FET turning-on 0.7 ns before the bottom FET. PSpice predictions show that this results in an asymmetrical pulse with a faster rise-time and slower fall-time: if the FETs are all triggered coherently then the predicted pulse is symmetrical. Triggering the FETs, in the 100 Ω stack, in sequence, starting at the top of the stack, such that there is 0.3 ns between FETs turning-on, compensates for the $\sqrt{L \cdot C}$ (0.3 ns) delay between levels: hence the rise-time is faster (5.2 ns predicted, 10% to 90%) but the fall-time is longer. If the order of the timing is reversed (−0.3 ns in Fig. 5) then a shorter fall-time can be achieved, with a longer rise-time (6.7 ns predicted, 10% to 90%).

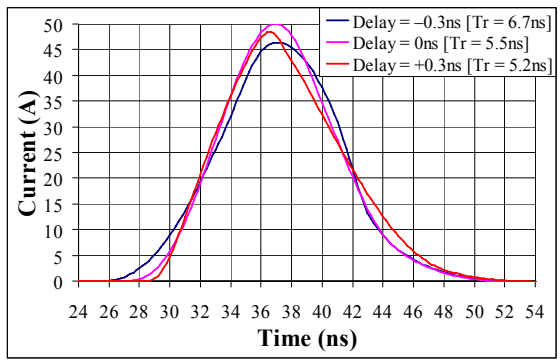

Figure 5: Predicted load current with −0.3 ns, 0 ns & +0.3 ns delay between adjacent FETs for 12.5 kV DC.

Conclusion

Pulses of 4.8 kV, with 4.3 ns rise and 5.5 ns fall, 10% to 90%, and a width of 13.7 ns at the 5% level have been generated at 60 kHz continuous: the post pulse ripple is <±5%. This is very close to meeting the specifications for the widest (14 ns), 2005 baseline, ILC pulses. The pulse rise-time and width can be further reduced by decreasing the stack inductance, by reducing the FET spacing, and by increasing the gate drive. Fast, higher voltage, FETs would also reduce the delay of the stack and hence the rise-time and width of the pulse. To allow adequate time to recharge the stack capacitance, improved fibre optics are required for the 3.25 MHz burst mode so that the FETs can be turned off within 50 ns or less.

REFERENCES

[1] G.F. Dugan, Private Communication, TRIUMF Meeting Nov. 1, 2005.

[2] M.A. Palmer et al., "Tests of a High Voltage Pulser for ILC Damping Ring Kickers", To be Publ. Proc. EPAC'06, 26-30 June 2006.

[3] M.J. Barnes et al., "Design of the Modulator for the CTF3 Tail Clipper Kicker", This conf.

[4] R.B. Armenta, M.J. Barnes & G.D. Wait, "Precision 25 kV Pulse and RF Suppression in a 75 kHz Kicker", 15th IEEE Int. Pulsed Power Conf., June 13–17 2005, Monterey, USA, pp676-679.

[5] M.J. Barnes & G.D. Wait, "A 25 kV, 75 kHz, Kicker for Measurement of Muon Lifetime", IEEE Trans. Plasma Science, Vol. 32, No. 5, Oct. 2004, pp1932-1944.

[6] M.J. Barnes et al., "A High Frequency MOSFET Driver for the TITAN Facility at TRIUMF", Proc. 15th IEEE Int. Pulsed Power Conf., June 13–17 2005, Monterey, USA, pp178-181.