THE SNS MACHINE PROTECTION SYSTEM: EARLY COMMISSIONING RESULTS AND FUTURE PLANS*

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Abstract

The Spallation Neutron Source under construction in Oak Ridge TN has commissioned low power beam up to 187 MeV. The number of MPS inputs is about 20% of the final number envisioned. Start-up problems, including noise and false trips, have largely been overcome by replacing copper with fiber and adding filters as required. Initial recovery time from Machine Protection System (MPS) trips was slow due to a hierarchy of latched inputs in the system: at the device level, at the MPS input layer, and at the operator interface level. By reprogramming the MPS FPGA such that all resets were at the input devices, MPS availability improved to acceptable levels. For early commissioning MPS inputs will be limited to beam line devices that will prohibit beam operation. For later operation, the number of MPS inputs will increase as both software alarms and less intrusive MPS inputs such as steering magnets are implemented. Two upgrades to SNS are on the horizon: a 4 MW upgrade and a second target station. Although these are years away the MPS system as designed should easily accommodate the increase in power and pulse-to-pulse target switching at 120 Hz.

STARTUP PROBLEMS

Initial startup of the SNS front end and DTL was plagued by noise problems and false MPS trips which reduced beam availability for commissioning activities. The first warning sign came through the timing system when errors on the Real Time Data Link (RTDL) and Event Link (EL) showed numerous errors not only in the MPS system but the HPRF gates as well. Problems were quickly traced to a ground loop tying the RFQ ground to the MEBT ground plane through a timing system cable. After removing the ground loop, beam was available albeit with frequent nuisance trips. A program was initiated to study the EMI/RFI and grounding problems [1] which resulted in several conclusions which were implemented. The main point was to not allow cables with shields to cross "local grounding planes", which are based on the high power RF grounding boundaries. These are defined as the local grounding boundary.

Fiber Conversion

After initial problems were isolated to ground loops, EMI and RFI interference we changed the baseline design to all fiber for any cables traveling outside the local grounding area's. In retrospect, this should have been the baseline design from the beginning but this was carried through from "experience" at other labs where there were minimal noise problems in these systems. Fiber repeaters have been designed and installed to replace copper fanout^{*} units. The MPS chassis and PCB's were modified to accept fiber instead of copper. Input chassis designed to convert contact and non-standard MPS inputs were modified with filters on the inputs to minimize noise impacts on the inputs. The inputs using these are slow inputs where the additional millisecond delay in response time does not impact the effectiveness of the MPS shutdown.

The results of these efforts have paid off. We went from 10's of false trips per day to zero. A false trip is defined as an MPS trip with no record of the MPS input device faulting, (through EPICS monitors).

MPS INPUT SUMMARY

The number of MPS inputs will double for the next commissioning run from the previous run. Table 1 shows the number of inputs anticipated for full power beam operation. Corrector magnets are wired to MPS but are not used during commissioning.

System *	1	2	3	4	5	6	7
BLM / ND		75	129	38	92	21	23
BS Coll							
Dump	2	6	11	10	12	8	8
Beam							
Instr	10	31	7	10	4	2	4
Power							
Supplies	25	96	90	35	192	13	28
Vacuum	6	9	14	4	2	1	2
RF Systems	10	30	102	2	36		
MPS	8	6	8	2	8	2	
Totals	61	253	361	101	346	47	65

Table 1: MPS input summary for post CD4 operations.

* 1 - MEBT-BS, 2 - CCL_BS, 3 – LDmp, 4 – Idmp, 5 – Ring, 6 – Edmp, 7 - Tgt

The LLRF system also provides MPS inputs. The hardware inputs include a vacuum OK, arc detectors, configurable trip levels for forward and reflected power, and cavity fields. A future input will be put into the FPGA to monitor the cavity amplitude and phase errors. Software inputs also trip the LLRF MPS input Signals through EPICS include heartbeats from HPRF, RCCS and

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Cryo IOC's. Chatter faults are monitored from the arc detectors and RF power inputs.

New Inputs for SCL Commissioning

For previous runs the MPS inputs were based strictly on the hardware status of devices. A power supply could be on, but set to any random value and MPS would be satisfied. All power supply focusing and bending magnets now have software MPS windows. The set point is taken from the accelerator physics Oracle database tables. The windows are initially set to +/5% for warnings and +/-10% for software trips. During commissioning these can be bypassed individually or in groups, associated with tuning the accelerator. Bypasses will not be permitted during high power operation.

The beam loss monitors have had very limited use to date for machine protection. The signals are filtered, and then integrated before the MPS comparator circuit. The signal level is dependent on the number of particles lost and beam energy (among other things). There is roughly an order of magnitude difference between the low energy and CCL sections of the SNS machine. The trip level for 100% beam loss into a faraday cup is ~20 mV / 5V at 180 MeV. The time for the integrator to reach this thresh hold is about 30 usec. Although the trip level is low, if the noise levels are minimized, this should not be a problem. The loss limit is 10⁻⁴ at 40 ma so commissioning at 1 Hz and 50 usec limits the maximum losses at 7.8×10^{-4} or 4.7×10^{-4} with the 30 usec detection time. Using the single shot feature or N pulses per shot, the beam loss should be below 10^{-4} .

The BLM's were cross calibration with TLD's during the last run. This should allow proper trip points and integrated loss in terms of RADS for the upcoming run.

Other Inputs

The Differential Beam Current Monitors have not been useful to date. Noise from the ION source 2 MHz and 13 MHz amplifiers, as well as 60 Hz noise has made this system inoperable from the MPS and accelerator availability point of view. Work is in progress to decrease the noise generated from the source. The toroid cores are grounded at the beam-line making ground loops a problem. Differential receivers in the analog front end electronics of the beam current monitors and digital signal processing should help eliminate these problems.

Studies have been conducted on the expected beam loss in the ring if the injection kickers are not available [2]. If all kickers failed (IOC failure) most of the beam would be lost in the ring. Timing system heartbeats at 60 Hz will detect this type of failure when the IOC is installed with MPS hardware. The present ring design has all MPS inputs in dedicated IOC's. An independent monitor with triggers and data from the RTDL is needed to guard against this situation. The painting scheme also depends on all 8 injections kickers operating in tandem. A fairly simple comparator circuit can be built to monitor the waveform currents against "standard" library waveforms.

MACHINE AVAILABILITY

Latched Inputs

Latched inputs are for devices that need a manual intervention to restore that device to a particular state. Auto reset devices can return to a satisfied state for the next beam pulse. Initial implementation of the latched inputs required three MPS resets plus the input device itself which made an MPS trip cumbersome to operations. These resets could have been ganged together in software but that would keep redundant features in place and could cause problems in the future with auto recovery routines. We decided that the input device latch is sufficient for all present MPS inputs so the feature was removed from the FPGA logic. The beam is still latched off after a fault so the beam does not turn on until devices are in a recovered state, meaning power supplies have been cycled, RF systems are stable, etc. This reduced the number of operator screens required for recovery from an MPS trip from up to 6 to 2 or 3.

MPS SOFTWARE TOOLS

Post Mortem

The post mortem application is a first fault diagnostic at this time. There are four MPS events broadcast on the timing system Event Link (EL). Three relating to post mortem are the fast protect latched (FPL), fast protect auto reset (FPAR), and fast protect, diagnostic event. The FPL event is used to trigger circular buffer archive records. These are inputs that should change slowly in time with respect to the maximum beam rate. The FPAR events trigger circular buffers from beam diagnostics and LLRF systems that can change within a pulse. These can also be used to trigger transient recorders of commercial instrumentation, high speed oscilloscopes, real time spectrum analyzers, etc. In order to keep the amount of data archived to a reasonable level, the third trigger is throttled to 6 Hz, which is programmable.

High level applications are needed to absorb this data and present it to operations in a reasonable fashion.

Mode Mask Verification

Mode masking is required to allow pilot beams during commissioning and accelerator startup for intrusive diagnostics to be inserted. Pilot beams will also be used after machine downtimes before bringing the accelerator up to full power. After proper beam transport is verified, the beam mode is changed and masks are removed. Improper configuration control over theses masks and configuration files could result in machine damage and excessive machine downtime.

An ORACLE RDB application defines default masks based on the device type. For instance wire scanners are allowed in the beam if the pulse width is less than 50 usec. Beam is shut off to protect the wire scanner if a longer pulse is requested. Changes to the default modes are logged into the SNS e-log system. An application program also reads the mode masks from the RDB and verifies the hardware configured mode masks. This is required for all startups of the accelerator after shutdowns or long maintenance periods. Any discrepancy between the RDB configuration and the MPS hardware configuration is logged in the e-log. The procedure is a part of the startup procedure for SNS.

Input Status for Mode Changes

In order to efficiently change between beam stops or dumps, an MPS mode view application has been written. This allows operations to see what will trip the beam before changing machine modes. As commissioning activities are completed the next section of machine can be readied for beam. These inputs are masked from the alarm system so the "green screen" concept can be implemented. Figure 1 shows inputs that will trip the beam in red, inputs that will conditionally trip the beam in blue, and inputs that are satisfied or mode masked in black.

MPS System Verification

An important part of the turn on sequence before commissioning or after a maintenance period is the verification of the MPS input status. Maintenance periods often require bypasses installed for local system testing. A quick verification enhances the MPS reliability; will MPS shut off the beam if required? A program is under test that forces each input to a faulted state and verifies an MPS fault. The goal is a complete verification in less than 4 hours.

X MPS Input Status Verificati File Edit Special View Wind	on – Br ow He	owser Ip					= O X					
CCL BS Input Status												
RTDL Switch												
		tandBu	CtandD									
	3	CL BS	CCL BS									
Src Input Status		CL_BS Inp	out Status		LDmp Input Status							
IDmp Input Status		Ring Input Status			EDmp Input Status							
Tgt Input Status												
MDC DV		Innut St	100500	E Ou Cos	1000500	1	FullDurg					
DTE_Vac.DOVD.TTE_CCE_DD_IIIII		v	VIOUSEC	SOUSEC	VUUUSEC	TWPEC	FUIIPWE					
DTL_Vac:SGV6:FPL_CCL_BS_mm		0	0	0	0	0	0 -					
SCL_Mag:PS_QH00:FPL_CCL_BS_mm		0	0	0	0	0	0					
SCL_Mag:PS_QV00:FPL_CCL_BS_mm		0	0	0	0	0	0					
CCL_Diag:WS310:FPAR_CCL_BS_mm		0	1	1	0	0	0					
CCL_Diag:WS406:FPAR_CCL_BS_mm		0	1	1	0	0	0					
DTL_Diag:FC160_out:FPAR_CCL_BS_mm		0	1	1	0	0	0 =					
DTL_Diag:FC428_out:FPAR_CCL_BS_mm		0	1	1	0	0	0 -					
DTL_Diag:FC524_out:FPAR_CCL_BS_mm		0	1	1	0	0	0					
DTL_Diag:WS248:FPAR_CCL_BS_mm		0	1	1	0	0	0					
SCL_Diag:WS00:FPAR_CCL_BS_mm		0	1	1	0	0	0					
CCL_Diag:BLM00:FPAR_CCL_BS_mm		1	0	0	0	0	0					
CCL_Diag:BLM101:FPAR_CCL_BS_mm		1	0	0	0	0	0					
CCL_DIAG:BLM102:FPAR_CCL_BS_mm		1	0	0	0	0	0					
CCL_DIAG:BLM103:FPAR_CCL_BS_mm		1	0	0	0	0	0					
CCL_DIag.BLM104.FPAR_CCL_BS_mm		1	•				· •					

Figure 1: Input status check for minimizing the time to change beam or machine modes.

Master Timing Pattern Generator

The Master Pattern generator is actually part of the timing system but it has implications for MPS [3]. Beam power constraints come from the MPS machine and beam mode. The beam scheduler should assure that the scheduled beam power does not exceed the beam dump power limits. Beam diagnostics are mode masked at small beam widths to allow beam. Insertion of a device at long pulse widths will trip the beam.

During DTL and CCL commissioning we were limited to 50 usec at 1 Hz. For the upcoming SCL commissioning this restriction will be lifted, but the average power to the dump has to be less than 7.5 kW. So in long pulse mode, the beam rep rate will be adjusted through the beam scheduler to keep the beam power within limits.

FUTURE UPGRADE CONSIDERATIONS

With the inherent risks of a 4 MW average power beam upgrade, some pulse to pulse verification of the beam parameters will be required. This will utilize MAID (Maximum Allowable Intrapulse Difference)[4]. This will mean an upgrade to existing beam diagnostics for 60 Hz beam information or possibly some dedicated BLM's, BCM's, and BPM's for MPS.

If a second target station is built, pulse to pulse mode mask changes will be required with two customers for beam. This will be tested well in advance using single turn injection interleaved with full power beam to monitor the injection phase space schemes. Timing system upgrades may be needed. A prototype system is being purchased for use with the 3D laser monitor.

CONCLUSIONS

The scalability of the MPS system has not been an issue. Inputs for each machine mode chain have risen from 10's to 100's. The delay through the MPS chassis has been minimized by making the hardware flow a branch input structure versus an interlock chain. The RDB has proven to be a reliable mechanism for adding new inputs with sufficient configuration control for the MPS system.

During commissioning MPS has been flexible enough to add or delete inputs as required. Mode masking has been stable and configuration files haven't been changed. Hardware bypassing has been minimized to 8 cases where hardware has been removed or added during this period. Software mask permissions have not been changed, although it is anticipated the permissions will be tighter as power is increased.

Reliability (devices installed, not handed over) are being handled. Bypass requests have been used to track uninstalled equipment as required. The availability problems have been overcome by increasing our susceptibility to noise and improvements made to the HPRF systems to reduce their noise output.

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