SWITCHED REFERENCE PHASE LOCK LOOP (SRPLL)*

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Abstract

The Brookhaven National Laboratory Relativistic Heavy Ion Collider (RHIC) has two beam synchronous event links (BSL), one for each ring, which use the 28 MHz ring low level rf to distribute event codes synchronously with a precise phase relationship to the beam. During a cogging reset just before injection, the low level rf sine wave is interrupted which causes the BSL receivers to lose lock. Lock loss in turn causes false triggers and other undesirable effects on the beam position monitors (BPM), ionization profile monitors (IPM), the tune meter and various experiments which use the BSLs. To rectify these problems, a SRPLL has been inserted between the beam synchronous master and the low level rf source. The SRPLL inserts a frequency and phase continuous splice over the dead-band gap in the rf source created during a cogging reset. The splice removes the gap and prevents the distributed BSL receivers from losing lock.

1 OBJECTIVE

The primary purpose of the SRPLL is to replace the lost 28 MHz RHIC low level rf signal during the cogging reset in a frequency and phase congruous manner to minimize excursions that could unlock the many PLL receivers connected to the beam synchronous systems.

Another purpose is to isolate the low level rf systems from the beam synchronous systems to allow synthetic clock and revolution ticks to be generated when low level rf systems are not available. This is especially useful when systems are developed, debugged, maintained, or installed during down time or maintenance periods. Any frequency from injection to storage can be delivered on demand for simulated proton or heavy ion runs.

Another purpose of the SRPLL is to produce a low jitter LVPECL digital clock from a 0 to +10 dBm low level rf sine wave to drive the beam synchronous master while controlling the phase relationship of the regenerated revolution tick to avoid setup and hold violations. If setup and hold violations occur on the SRPLL input, a sync error indicator flags the condition so that length adjustments can be made to the cable from the synchro synthesizer. Violations must not occur with frequencies from injection to storage. The SRPLL is designed to operate from 26 to 30 MHz which covers low energy heavy ion to fast proton injection frequencies.

Another purpose of the regenerated revolution tick is to guard against input revolution ticks spaced less than 1 revolution period apart after a cogging reset which cannot be tolerated by the BPM system.

2 BEAM SYNCHRONOUS SYSTEM

Two beam synchronous systems [1,2] distribute events synchronously with a fixed timing relationship with respect to the 360 rf buckets in each ring which may be selectively filled with ion bunches. The beam sync system is designed to work with flexible fill patterns. Fill patterns are referenced from the bucket 1 fiducial, named the revolution tick. The cogging reset is an asynchronous reset sent to the direct digital synthesizer (DDS) in the RHIC low level rf synchro synthesizer to align RHIC bucket 1 with the Alternating Gradient Synchrotron (AGS) for single bunch injection. It causes a 500 μs gap in the 28 MHz low level rf sine wave driving the SRPLL

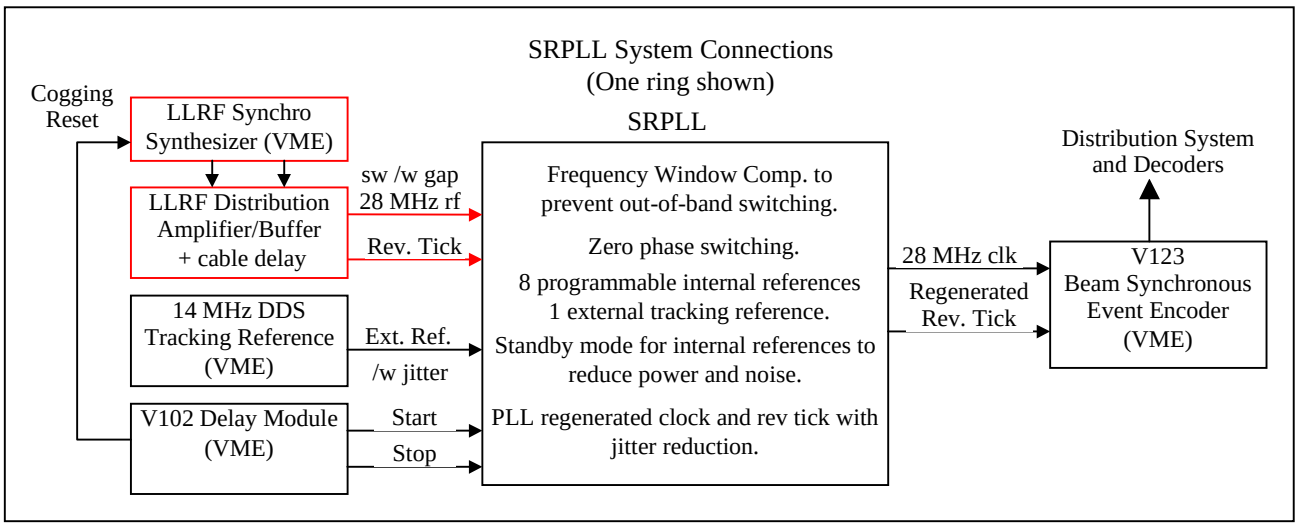

Fig. 1: SRPLL Interconnections

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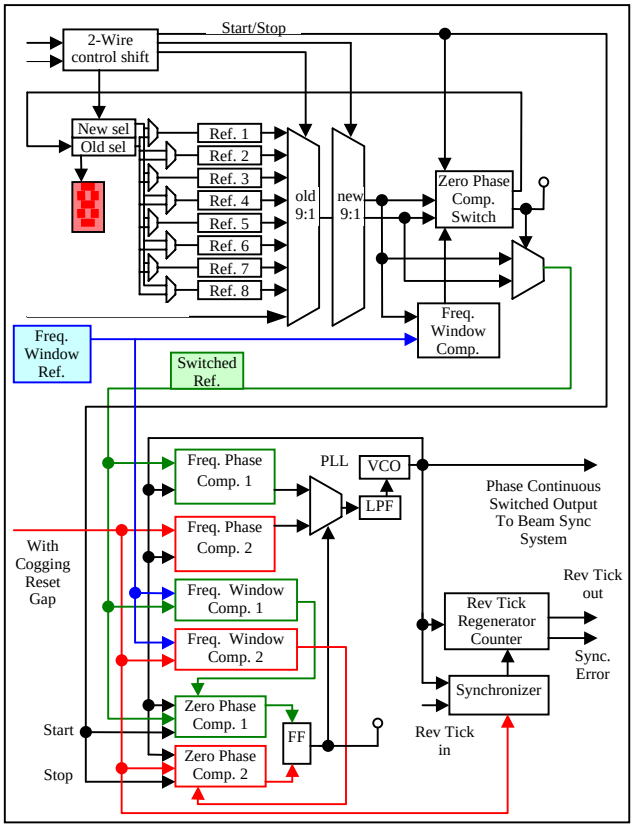

Fig. 2: SRPLL Block Diagram

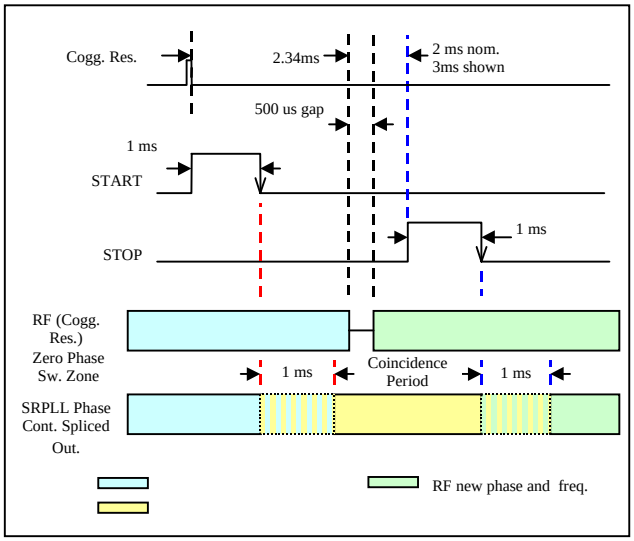

Fig. 3: SRPLL Timing

which drives the beam synchronous event system. (see Fig. 1) The cogging reset occurs just before beam is injected, so the BPMs and the IPMs which are using the beam synchronous systems would lose just prior to injection without the elimination of the reset gap.

3 SRPLL ARCHITECTURE

The SRPLL is comprised of several similar functional building blocks integrated into a single board level design. These blocks are: A two wire shift register control section, a phase lock loop (PLL), 8 switched internal frequency references with low power/noise standby, 1 external DDS tracking reference, several zero phase comparator switches, several frequency window comparators, a revolution tick regeneration counter, and status indicators. The SRPLL block diagram (Fig. 2) illustrates the interconnections. Complex control system functions that require VME bus access such as the tracking reference DDS are connected externally to isolate these from the noise sensitive SRPLL components. The jitter on the external DDS was a concern so the eight internal programmable frequency references were added. Later testing of the SRPLL with the DDS revealed enough jitter reduction for it to be used most of the time. Using an internal reference is better when the machine is idle and the DDS has nothing to track. Internal linear regulators are used with RFI filter studs on the enclosure to bring in clean power. Transformer isolation is used on inputs and outputs where practical. The zero phase matching of the input signal to the references requires a small footprint for the least delay and best phase alignment. The low jitter requirement of the BSL clock requires EMI/RFI shielding be employed in the SRPLL. All SRPLL components are integrated into a single printed circuit board (PCB) and sealed in an EMI shielded enclosure with SMA bulkhead connections going to 50-ohm cables terminated at the point of application on the PCB.

3.1 Frequency Window Comparators

The frequency window comparators work with a reference frequency to create an upper and lower frequency threshold that will inhibit switching into disconnected, unavailable or improper references. A frequency delta between the reference and the input signal, which is too large, will cause a large transient on the voltage controlled oscillator's (VCO) control input which can result in lock loss. Also, the PLL low pass filter is designed to minimize jitter, not to maximize agility, so the maximum frequency delta is constrained for these purposes by the frequency window comparators. On the other hand, too much constraint on the frequency delta will take too long for zero phase matching. Depending on system design parameters, the delta is selected within desirable limits, and the digital comparators are programmed accordingly. The SRPLLs in RHIC are using about a 1 kHz offset to guarantee switching within a 1 ms phase matching or coincidence period. (see Fig. 3)

3.2 Zero Phase Comparators

The zero phase comparators trigger within about 100 picoseconds of a phase match or rising edge coincidence between the two inputs. This signal is used to initiate the switch between the input and the reference. Zero phase is required when switching into and out of the reference to avoid phase errors which also appear as transients to the PLL phase comparators. Keeping the phase difference as small as practically achievable will aid in keeping the BSL as stable as possible during the switching periods.

The SRPLL switching characteristics are illustrated in Fig. 3. Note that the stop timing pulse is delayed more than is required for illustration purposes. Pulse widths, and spacing are variable depending on application.

3.3 Control Interface

The control interface implements start, stop and reference selection with choice of 8 internal reference frequencies or the external DDS reference. The reference selections are made via a serial pulse train into the start and stop controls, where the pulses overlap with one phase for 1 bits and the other phase for 0 bits. Pulses that do not overlap are start or stop pulses. The V102 delay module interfaces with the RHIC control system and is configured for the appropriate pulse widths and phasing to create the serial pulse train. Normal switching operation is automatic on the cogging reset event. (see Fig. 3)

3.4 Revolution Tick Regenerator

The revolution tick regenerator is a modulus 360 counter that is synchronized to the SRPLL output. A revolution tick from the synchro synthesizer sets the phase of this counter. Should the revolution tick be discontinued the counter will continue at the last known phase. After a cogging reset, the new revolution tick phase will be adopted if more than one revolution period has transpired. The RHIC revolution period is about 12.7 μs with a 28 MHz low level rf source.

4 RESULTS

A scope picture shows the results obtained. The top yellow trace is the low level rf source with a cogging reset gap. The second black trace from the top is the SRPLL output. The third red trace is the zoom in of the beginning of the cogging reset gap. The fourth blue trace is the zoom in of the SRPLL output. The green trace is the start pulse. The last blue trace is the stop pulse. (see Fig. 4)

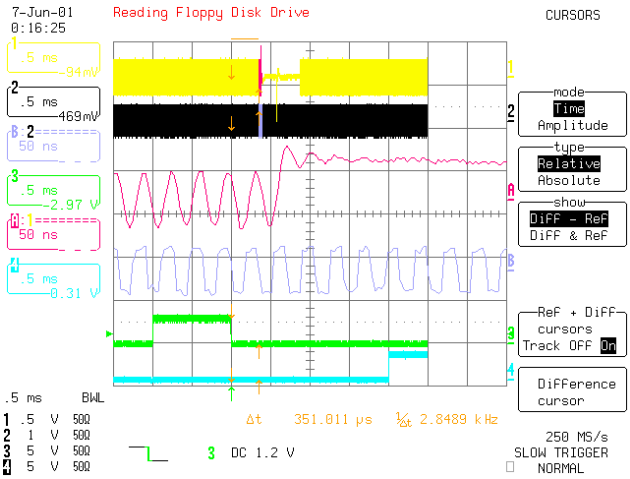

Fig. 4: SRPLL Scope Picture

5 CONCLUSION

The combination of the frequency window comparators and zero phase comparators with the PLL and references provided a solution to the cogging reset discontinuity in the RHIC beam synchronous timing. Switching within limits is now reliable and consistent, and has no observable consequences on the BSLs.

6 ACKNOWLEDGMENTS

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7 REFERENCES

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