THE ACCELERATOR PROTECTION SYSTEM BASED ON EMBEDDED EPICS FOR J-PARC

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Abstract

There are the 4 output beam lines at the Main Ring(MR) in J-PARC. The Accelerator protection system (MR-MPS) watches the devices which deal with destination of the beam. Then, the complicated logic judgment carries out using FPGA (Virtex-4 FX). On PowerPC core in the FPGA, LINUX+EPICS is operated. Though there are both logic processing unit and CPU on one element, the information transfer in high speed between logic processing part and CPU is possible without requiring the complicated external wiring. In this reason, the system can be very efficiently constructed. This paper describes the detail of the design and the implementation, as well as the experiences of the system in the operation of the J-PARC MR.

INTRODUCTION

At the J-PARC which is the high intensity accelerator, the operation is immediately stopped, when the abnormality arose in the equipment. Then, the beam in the accelerator is abandoned to the dump line. The activation of the component of the accelerator is prevented by this operation, and degradation and trouble are prevented. For such reason, the major equipment outputs the MPS(machine protection system) signal. The other MPS signal source : beam loss[1] and uncontrollability in LLRF. At the initial stage of the design, it was reported that there was sufficiently the time which disposes of the residual beam, after the head of the beam loss was detected. Based on the report, system design was carried out in order to respond by the whole MPS equipment in about 10 microseconds.

Except for the problem of the response speed, it had to be able to appropriately deal with addition and deletion of power supply. The MPS takes in one destination information of the beam, and the equipment which does not affect the beam is decided by it. The function which decided beam shutdown and beam disposal by excluding the signal of that equipment from the logic, was included in the MPS.

This report is an outline of the MPS system of MR of J-PARC which satisfies a demand of the description in the front.

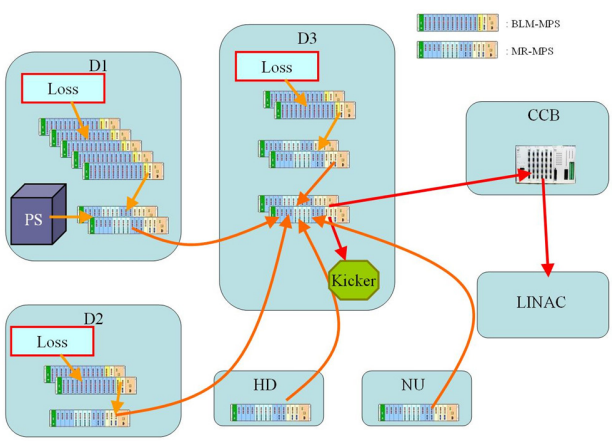

Figure 1: Arrangement and connection of the equipment.

GOAL

There were three large goals in the construction of the MPS of MR of J-PARC. The first is a speed of the logic processing. As several decade microseconds are tolerances by the whole system. Delay time of kicker power supply and for transmission hour in electric power line were also necessary, and then, the processing time by the whole MPS equipment was made to be 10 micro second as desired value. The processing time in one power supply building was made to be about 1 micro second as desired value, because 3-4 micro second were necessary for signal transmission between power supply buildings.

Another goal is to flexibly correspond for the change of the accelerator. In the initial stage of the operation of the accelerator, the frequency of abeyance of the equipment is high. It appropriately deals with the change, and it is necessary to enable the operation of the accelerator. In addition, there are many matters which cannot perfectly decide in the design, because the equipment as an target is abounding. Then, though it became important that logic and function could be changed after the manufacturing of the hardware, it became realizable by using the element of FPGA and CPLD.

By uniting logic processing unit and CPU and network, it was also one of the purposes to show that the system construction can be simplified.

HARDWARE

The MR accelerator of J-PARC has the 3 power supply buildings, and there is respectively a local control room. There are 2 beam lines for physics experiment in MR : Hadron (HD), Neutrino (NU). The signal is judged in experiment area and every power supply building, and the result is sent to MPS equipment of third power supply building (D3). Arrangement and connection of the equipment are shown in Fig. 1.

Signals between each building are 2 kinds of shutdown signals and beams disposal signal. The logic of "disconnection situation of the signal wire is abnormal" was chosen. The beam disposal is realized by request to

the kicker in D3. 2 kinds of shutdown signals which were double-tracked from D3 to central control building (CCB) are sent.[2]

The exclusive MPS equipment was designed in order to realize such function. It is adjusted to the type of input and output, because it becomes the modular construction, and it is possible to carry out various composition. The module for MPS(MR) is shown in Table 1. CPLD(XC95144XL) or FPGA(Virtex-4 FX) are being mounted on each module. For the reason, the change of the function is easy after the completion of the module.

The speed performance is important for the beam disposal. The result of 0.8 micro second was obtained, when the integrated processing time for the signal transmission of three steps was measured, (Fig. 2). It was 3-4 microseconds, when the transmission time by the cable between buildings was measured. They are about 10 microseconds in the time from the abnormal occurrence time to the beam disposal request time.

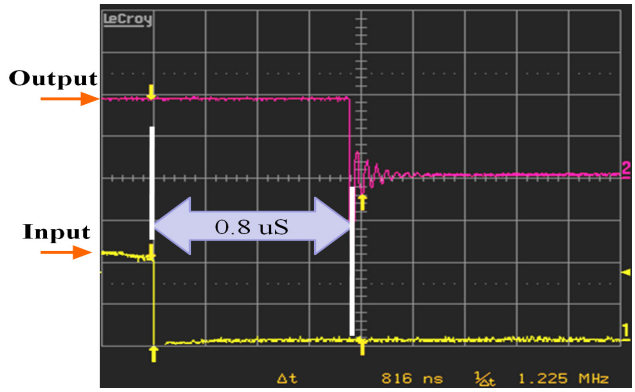

Figure 2: Time of signal transmission of three steps.

SOFTWARE

The logical operation of the MPS is directly carried out by both logic circuit of CPLD and FPGA. A CPU core included in the FPGA is not concerned in the logical operation of the MPS. However, CPU is very important in order to carry out management of the register of condition setting for the logic judgment and situation monitoring of the MPS.

LINUX was moved on CPU in order to simplify that work, and then, it managed IOC of EPICS. IOC watches the action of the MPS by 2 kinds of methods. The first is the direct monitoring of input-output condition of the MPS signal of the FPGA. The second is to read input-output situation of the module and setting situation of mask SW. It reads through the bus line in the backplane of the sub rack in the polling (Fig. 3).

In order to drive the accelerator, when either some kind of equipment broke down or the power supply was stopped for the research. By putting the mask on each signal, a stop output would not be issued under the abnormal situation. It is possible that efficiency of utilization of the accelerator is improved, if it can quickly deal with this operation. This MPS equipment has 2 kinds of mask functions.

One is SW in the input-output module. SW is used for the mask of the unused input channel.

The logic processing unit in the FPGA contains another mask. There are three registers which realize the function in the every input line: destination, timing, stop/disposal. In MR of J-PARC, there are 4 beam lines which send out the beam. The one destination control register is composed of 5 bits, which are 4 bits which show each beam line and 1 bit of the specialized function. It has the register of 8 bits in order to control the timing of the stop/disposal. The MPS equipment can output 8 channels. It has output control register of the 8 bits which chooses output channel which decides the stop/disposal. The connection of the register for the mask is shown in Fig. 4.

Table 1: Parts for MPS (MR)

Application purpose.	Type	Name	ID
MR-MPS/Abort	Backplane	MR-MPS-BUS	
	Relay signal input	MR-MPS-OPT	2
	Optical signal input	MR-MPS-OLC	3
	TTL signal input	MR-MPS-TTL	4
	Long distance optical transceiver	MR-MPS-FCT	1
	TTL or Relay In/Out	MR-TTL-GIO(TTL/Relay)	5/6
	CPU(IOC)	MR-MPS-CPU	
	Power Supply	MR-MPS-POWER	
MR-Loss	Backplane	BLM-MPS-BUS	
	TTL signal input(8 Input)	BLM-MPS-TTL	8
	Relay signal input	BLM-MPS-OPT	7
	Long distance optical transceiver	BLM-MPS-FCT	9
	CPU(IOC)	BLM-MPS-CPU	
	Power Supply	BLM-MPS-POWER	

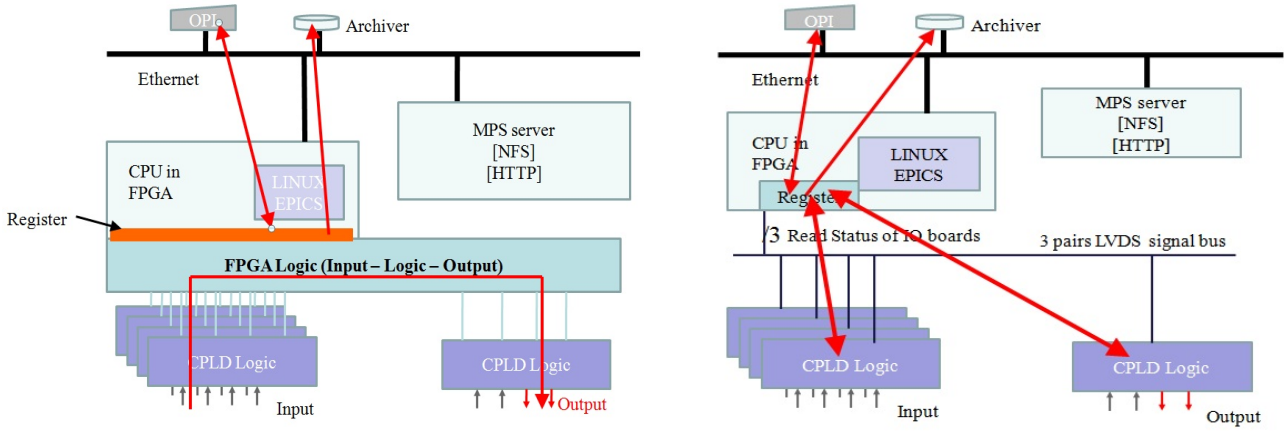

Figure 3: Two types of register and signal flow of MR-MPS.

OPERATION RESULT

Though it is the work of the MPS to prevent activation and degradation of the equipment, the operation will be inhibited when the malfunction is caused. In the reason, the high reliability is required so that it may not become the hindrance of the operation. It is important that it does not inhibit the operation, because the beam from the RCS is used even in the MLF area. The MPS of MR becomes about 500 hours, after the experimental real operation is done. The phenomenon of the MPS which arose in this period was shown in Table 2.

Initial failure and illegal operation were detected enough. There was once the report of "the MPS issued the stop signal, though there was no equipment abnormality". The phenomenon did not reappear, when it was investigated. The phenomenon which might become a cause of the malfunction of the MPS was not found either. It was possible to accurately catch the abnormality of the equipment except for it.

CONCLUSION

The goal of "the time until it issues the disposal and request from the malfunction detection is 10 micro second or less" had been made, and it was able to be realized hoop. However, there is a problem in the kicker power supply, and countermeasures are necessary.

The logic is directly carried out by the FPGA, status management and mask management are carried out in EPICS on a CPU core, such composition was chosen. By separating two functions, expecting above softness was

Table 2: Operation Summary

Month	Operaton (h)	Shot	Devices	Frequency	Malfunction
Jan.	117	630	11	61	0
Feb.	87	5194	4	6	0
Apr.	81	2955	13	13	0
May	95	2764	5	13	1
Jun.	122	3484	2	2	0
Total	502	15027	35	95	1

The report of misoperations and equipment tests etc. is not counted.

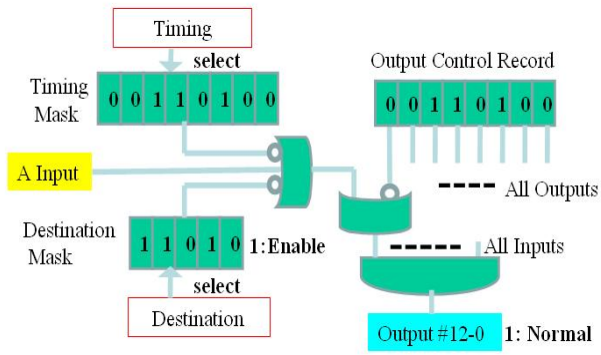

Figure 4: Signal Masks.

able to be realized, while the sufficient processing speed was ensured. The wiring became very simple, because two functions were realized in one element.

Mask change of temporary measures is quickly possible in the drive downtime, when the sufficient consultation with the person concerned is done. The reliability would be heightened by 2 time confirmation work in the signal input part. There was the report of the nonconformity of equipment and MPS in the operation of about 500 hours only at the once. It did not reappear, even if the test was done for the confirmation. The reliability of the equipment is verified in future operation.

REFERENCE

[1] T. Toyama, "Beam Diagnostics for the J-PARC Main Ring Synchrotron", PAC'05, Knoxville, May 2005, p. 958 (2005); http://cern.ch/AccelConf/p05/PAPERS/RPAT005.PDF .

[2] H. Sakaki, "Current Status of the Control System for J-PARC Accelerator Complex", ICALEPCS'07, Knoxville, October 2007, p. 62 (2007); http://cern.ch/AccelConf/ica07/PAPERS/TOAB02.PDF .