APPLICATION OF EPICS ON F3RP61 TO ACCELERATOR CONTROL

J. Odagiri, S. Araki, K. Furukawa, N. Kamikubota, A. Kiyomichi, H. Nakagawa, T. T. Nakamura, K. Mikawa, S. Murasugi, S. Yamada, N. Yamamoto, KEK, Tsukuba, Japan
K. Kameda, T. Natsui, H. Shiratsu, Yokogawa Electric Corporation, Tokyo, Japan
M. Komiyama, RIKEN, Wako, Japan
S. Motohashi, M. Takagi, Kanto Information Service, Ibaraki, Japan
N. Nagura, Nippon Advanced Technology Co., Ltd., Ibaraki, Japan
T. Nakamura, Mitsubishi Electric System & Service Co., Ltd, Tokyo, Japan
A. Uchiyama, SHI Accelerator Service Ltd., Tokyo, Japan

Abstract

A new type of Input / Output Controller (IOC) has been developed based on F3RP61, a CPU module of FA-M3 Programmable Logic Controller (PLC). Since the CPU module runs Linux, it takes no special effort to run EPICS IOC core program on the CPU module. With the aid of wide variety of I/O modules of FA-M3 PLC, the F3RP61-based IOC has various applications in accelerator controls, such as magnet power supply control, stepping motor control, data acquisition from beam monitors, monitoring interlock status and so forth. The adoption of the new IOC makes the architecture of accelerator control systems simpler by unifying the two layers of front-end computers, i.e., the IOC layer and the PLC layer, into one layer. We found that the simplification of the control system architecture helps us to reduce the time and cost for the development and maintenance of application software.

INTRODUCTION

Modern accelerator control systems are adopting more and more PLCs as their front-end controllers. In EPICS-based control systems, they are usually connected with IOCs through Ethernet and supervised by the IOCs over the network (Fig.1 (A)). This configuration is reasonable when the programming needs to be divided into PLC's side and IOC's side in order to allow non-EPICS-experts to share the programming by using ladder programming languages, which are popular to engineers in the industry. This is particularly the case when we have companies implement local control logic for their products, such as magnet power supplies and so forth.

On the other hand, if all of the programming is carried out by programmers who have already been experienced in EPICS, having yet another front-end controller (PLC) under a front-end controller (IOC) pointlessly increases the workload from the following reasons. 1) Learning ladder languages and their development environments becomes additional burden. 2) Control logic distributed over PLCs and IOCs makes trouble-shooting harder. 3) Communication between PLCs and IOCs requires complicated asynchronous device/driver support modules.

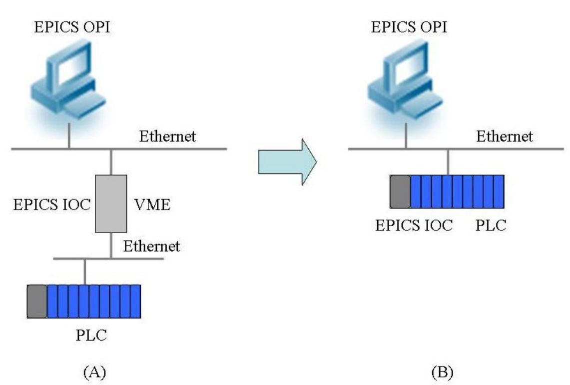

Figure 1: Consolidation of front-end computers.

EPICS ON F3RP61

Recently, PLC CPUs that run a real-time Operating System (OS) became available on the market to open the way to executing iocCore directly on the CPUs. By using PLCs themselves as IOCs, as shown in Fig. 1 (B), we can make the structure of our control systems flatter and simpler to solve all the problems mentioned above [1]. 1) Learning ladder languages and their development environments is no more required. 2) Control logic concentrated on an IOC makes trouble-shooting easier. 3) Device/driver support can be implemented just by wrapping Application Program Interfaces (APIs) of Board Support Packages (BSPs) to be supplied with the CPU modules.

Among this kind of CPUs, Yokogawa F3RP61 (Fig. 2), which functions with I/O modules of FA-M3 PLC,

Figure 2: F3RP61 in operation.

features Linux support. For accelerator control systems, which are frequently updated throughout their lifetimes, it is of importance to reduce the time and cost required for the development of application software. The adoption of Linux for IOCs meets the requirement since developing programs in the user-space is easier and quicker than doing it in the kernel-space. Large improvement of real-time performance of Linux kernel in recent years is another reason for choosing Linux. With the kernel pre-emption feature enabled, F3RP61 has reasonably good real-time responsiveness that can satisfy control needs in many cases.

After feasibility tests carried out in the spring of 2008 to confirm that F3RP61 can fully function as IOC, F3RP61-based IOCs were adopted for EPICS-based control systems of KEKB, J-PARC and RIKEN RI Beam Factory [2], [3]. Since then, they have rapidly been applied to several different accelerator control purposes.

APPLICATIONS

This section describes some of the examples of F3RP61-based IOCs in operation at KEK.

Magnet Power Supply Control

Recently, PLCs tend to be adopted as the embedded controllers of relatively large-scaled power supplies for powering magnets and RF sources. An F3RP61-based IOC can be used as their dedicated controllers if an EPICS expert takes the charge of the programming. In this case, the sequence logic to operate the power supplies can be programmed by using EPICS sequencer written in Sequence Notation Language (SNL). Having the notion of state and the "when" clause to wait events, SNL allows us to write easy-to-read and easy-to-maintain programs.

F3RP61-based IOCs were first applied to control power supplies for the pulsed quadrupole magnets of the KEKB Main Ring, which is used to adjust tune shift [4]. F3RP61-based IOCs replaced existing ordinary PLC's CPUs running ladder programs with remaining all the other I/O modules in the existing PLC unit unchanged. A conditional ramping, which means changing output voltage quickly or gradually depending on whether it is higher or lower than a threathhold value, was implemented by using an EPICS sequencer program in a clear and simple manner to make the maintenance work easier.

The control subsystem of the J-PARC slow extraction line also adopted F3RP61-based IOCs to control the power supplies for the electrostatic septa and magnetic septa [5]. Since existing old power supplies were recycled for all magnetic septa, it is required to interface old PLCs embedded in the power supplies with the EPICS-based J-PARC control system. In order to avoid risks in reconstructing old but working system, F3RP61-based IOCs were added on top of the existing PLCs by connecting the I/O modules of the both controllers using metal cables to allow them to communicate each other.

Another application of the F3RP61-based IOC to power supply control can be found in reference [6].

Stepping Motor Control

Several different types of positioning modules for FA-M3 are available for an F3RP61-based IOC to control movable devices of accelerator components. In order to make the positioning module execute an action, such as positioning in one direction, searching for the origin, resetting the origin, etc., the IOC needs to execute a sequence of I/O operations on control registers of the positioning module. It also fits into the SNL expressions quite well. In applications in accelerator control, positioning of devices, in many cases, is done by moving multiple axes independently. Obviously, a single sequencer program associated with parameter substitution files describing the axes suites to the purpose.

The control subsystem of the movable beam masks of the KEKB Main Ring has been upgraded by replacing existing ordinary PLC's CPUs with F3RP61 CPUs [7]. Eight masks at two stations are controlled by an F3RP61-based IOC. Two out of four F3RP61-based IOCs have already been operated since the summer of 2008 without any troubles.

The control subsystem of the slow extraction line of the J-PARC Main Ring also adopted an F3RP61-based IOC for the positioning of its movable septa. The IOC executes positioning of the electrode and yoke of the electrostatic septa, a set of magnetic septa and a set of screen monitors installed in the extraction line. In total, seventeen axes are handled by using five positioning modules under the supervision of the IOC.

Data Acquisition from Beam Monitors

FA-M3 has analogue input modules with high speed ADCs which can reach up to the maximum conversion rate of 20 kHz. With this type of analogue input modules, F3RP61 can comprise an EPICS-based programmable data acquisition unit for relatively slow signals, such as beam signals pre-processed by their own dedicated circuits to process fast raw signals. A high speed digital module for FA-M3 PLC can also be used to accept external triggers to drive the data acquisition in synchronous with the beam. By developing a device support for the iocCore to access the I/O modules, a fully programmable data acquisition unit can be realized with ease.

F3RP61-based data acquisition has been adopted for two different types of beam monitors of the J-PARC Main Ring. One is the beam loss monitor, which comprises of more than three hundreds of gas chambers distributed along the ring (Fig. 3), and the other is a fast current transformer installed in the fast extraction line of the Main Ring. In both cases, the raw signal is integrated by a processing circuit and its output is read by an F3RP61-based IOC through an ADC channel. Although the two systems largely differ in the number of channels they handle, the basic function is the same in the regard that they read ADC channels driven by an external trigger coming from the timing system of the accelerator.

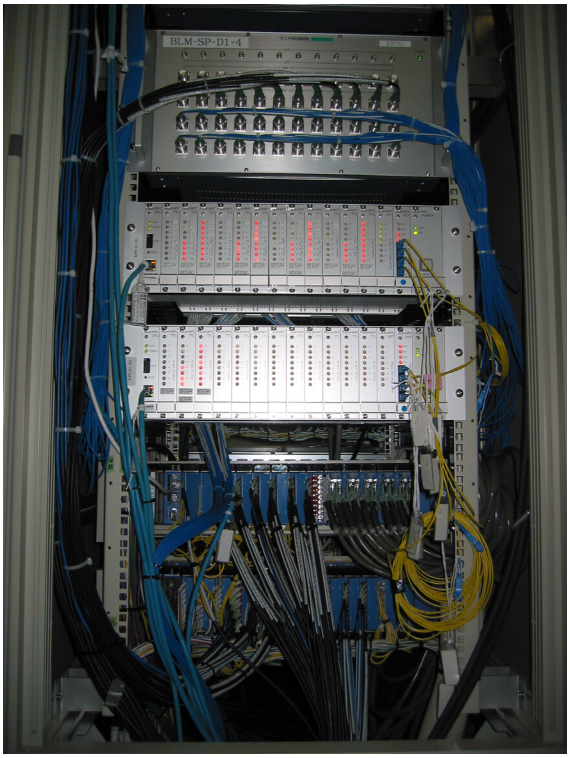

Figure 3: DAQ system for BLM of J-PARC Main Ring.

Real-time performance can be an issue for both systems. As to the beam loss monitor, the jitter of the data acquisition timing needs to be small enough to make it meaningful to compare the acquired data between the previous accelerator cycle and this cycle. The real-time requirement of the fast current transformer is attributed to the fact that the raw signal processing circuit holds valid output no longer than four milliseconds. The operational experience has showed that the F3RP61-based IOC can meet the requirements for both of the applications [8].

Interlock Status Monitor

PLCs are widely used in interlock systems for their reliability. Considering the fact that the logic to interlock devices is normally implemented by using simple combination of ANDs and ORs, which are graphically well expressed by real and virtual relays in ladder programs, there is little point in replacing an ordinary PLC's CPU with an F3RP61-based IOC. In interlock systems, F3RP61-based IOC can be best used in order to interface ordinary PLC's CPUs with an EPICS-based control system which should be monitoring the interlock status at a higher level [9]. It has been a common practice to connect an IOC with PLCs using Ethernet to monitor interlock status. In this case, it is crucial to read out the data as much as possible at once on one transaction by using waveform record because the message-based I/O on TCP/IP is a rather slow transaction.

The method to monitor interlock status, however, has a disadvantage in application development point of view. The interlock status transferred from PLCs to an IOC need, in the end, to be decomposed into each bit that indicates whether a relay is on or off. The standard procedure to decompose the data starts with first cutting out a group of sixteen bits from the waveform record by using subArray records. The data in a subArray record is then copied into a multi-bit binary record so that each status bit can be accessed by Channel Access (CA). In total, three layers of records are required to monitor the interlock status.

F3RP61-based IOC can solve the problem by working with the ordinary PLC's CPU side-by-side on the same unit. By sharing the same PLC-bus with the ordinary PLC's CPU, the IOC can have register-based access so that it can read the data much faster, possibly a hundred times or so, than when it reads the data over the network. As a result, the IOC is allowed to read the status data by word (sixteen bits) using multi-bit binary record from the beginning.

CONCLUSIONS

With wide variety of I/O modules, F3RP61-based IOCs have various applications in accelerator control, such as controlling power supplies and stepping motors, data acquisition from beam monitors and monitoring interlock status. Throughout the applications, the development and maintenance of application programs became quicker and easier owing to the consolidation of PLC's CPU and IOC into one F3RP61-based embedded IOC. The adoption of Linux as its OS played a key role to enhance the productivity in the software development.

REFERENCES

[1] J. Geyang *et. al.*, "Porting EPICS onto micro-ITRON/SH4-based Device Controllers", PCaPAC05, Hayama, Japan, March 22-25, 2005.

[2] A. Uchiyama *et. al.*, "Development of Embedded EPICS on F3RP61-2L", PCaPAC08, Ljubljana, Slovenia, 20-23, 2008.

[3] M. Komiyama *et. al.*, "Upgrading the Control System of RIKEN RI Beam Factory for New Injector", in this conference.

[4] K. Mikawa *et. al.*, "Embedded EPICS Controller for KEKB Pulsed Quadrupole Magnet Power Supply", in this conference.

[5] M. Takagi *et. al.*, "Control of the J-PARC Slow Extraction Line Based on Embedded EPICS", in this conference.

[6] S. Araki *et. al.*, "Magnet Power Supply Control Based on EPICS on F3RP61 for KEK-ATF", in this conference.

[7] T. Nakamura *et. al.*, "Upgrading the control System of the Movable Mask for KEKB", in this conference

[8] S. Motohashi *et. al.*, "Data Acquisition System of Beam Loss Monitors of J-PARC Main Ring", in this conference.

[9] Y. Sato *et. al.*, "Control System for J-PARC Hadron Experimental Facility", in this conference.