DIGITAL PHASE CONTROL SYSTEM FOR SSRF LINAC

C.X. Yin, D.K. Liu, L.Y. Yu, SINAP, Shanghai, China 201800

Abstract

In order to reach the requirement of RF phase stability, digital phase control system is implemented in SSRF (Shanghai Synchrotron Radiation Facility) LINAC, which has already operated since May 2007. FPGA is the key of digital phase control system, which contains digital I/Q demodulator (phase detector), digital I/Q modulator (phase shifter) and control algorithms. With the aid of FPGA, the whole period of closed-loop is about 40ns, and delay of closed-loop is about 1us. The preliminary testing result was presented in this paper.

INTRODUCTION

SSRF 150MeV LINAC includes a thermionic cathode electron gun, a 500MHz sub-harmonic buncher, a 2998MHz buncher and four accelerating sections. The accelerating section is constant gradient accelerating structure, and its working frequency is 2998MHz, six times of storage ring RF frequency.

The layout of SSRF LINAC is shown in Fig. 1. One klystron is used for the 2998MHz buncher and two accelerating sections; another klystron is for another two accelerating sections. Two solid-state power amplifiers drive two klystrons respectively.

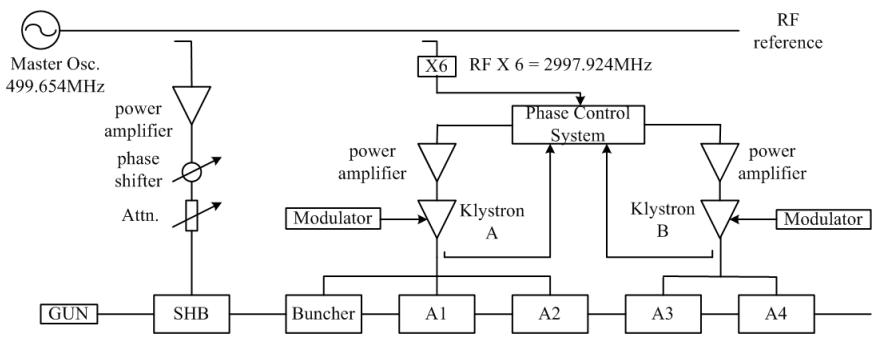

Figure 1:The layout of SSRF LINAC

In order to realize desired low energy spread in 150MeV LINAC, the requirement of phase control system is to control interpulse phase shift of klystron forward signal within ±1 degree [1].

SYSTEM DESIGN

The design philosophy of digital phase control system is list below:

- Implement passive coaxial RF component to down-convert RF signal to IF signal, and up-convert IF signal to RF signal.
- Implement commercial products for ADC, DAC and clock management modules.
- Implement digital I/Q demodulation as phase detecting algorithm, and digital I/Q modulation as phase shifter.
- Implement feed-forward control to compensate interpulse phase shift of klystron forward signal.
- Implement FPGA for signal processing and control.
- Implement embedded computer and real-time operation system for iterative algorithm calculation in feed-forward control.

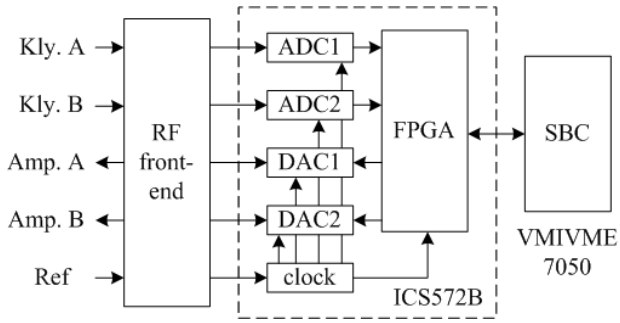

Figure 2: Layout of phase control system

The brief layout of digital phase control system is shown in Fig. 2. ICS572B is the PMC module, which includes two ADCs, two DACs, clock management, and FPGA [2]. VMIVME 7050 is the VME single board computer, used for iterative algorithm calculation.

RF Front-end

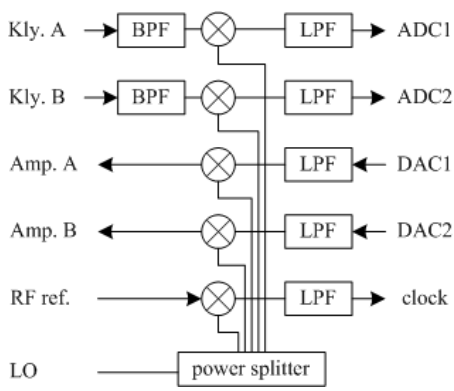

Figure 3: Layout of RF front-end

As shown in Fig. 3, two klystrons forward signal is down-converted to IF signal (25.6MHz), which are sampled by two ADCs respectively; two DACs outputs are up-converted to RF signal (2997.924MHz), used as power amplifier input; RF reference signal (2997.924MHz) is down-converted to IF signal (25.6MHz), used as input signal for clock management module in ICS572B.

Clock

To satisfy digital I/Q demodulation requirement, ADC sampling clock needs to be synchronized with reference IF signal, and DAC sampling clock also needs to be synchronized. Clock management module in ICS572B can generate five clocks synchronized with input signal, which have a high flexibility to the frequency ratio of input signal.

Clock management module consists of TI CDC7005, 409.6MHz VCXO, and passive filter for PLL. With the proper settings, clock management module generates two ADCs sampling clock (102.4MHz, four times of reference IF), two DACs sampling clock (204.8MHz, eight times of reference IF), and one FPGA clock (25.6MHz).

FPGA clock is used for sampling data alignment in digital I/Q demodulation.

Control includes feed-forward control and iterative algorithm calculation.

Digital I/Q modulation is already contained in DAC, and iterative algorithm calculation is done in software. So additional parts of signal processing and control need to be realized in FPGA.

FPGA

ICS572B includes a Xilinx Virtex-II FPGA (XC2V4000) that can be programmed by PCI bus. FPGA contains digital I/Q demodulation, I/Q to Phase conversion, feed-forward control, phase to I/Q conversion, DAC input data conversion.

To satisfy the phase stability requirement, the close-loop period of phase control system should be short as possible. Since the frequency of IF signal is 25.6MHz，we choose 40ns (1/25.6MHz) as close-loop period. So the data stream frequency of all parts mentioned above in FPGA must be more than 25.6MHz.

In addition to signal processing & control parts, FPGA needs to contain some registers and memory for data exchanging with software.

FPGA contains two identical channels that work simultaneously, and one channel controls one klystron forward signal's phase respectively. The layout of one channel in FPGA is shown in Fig. 4.

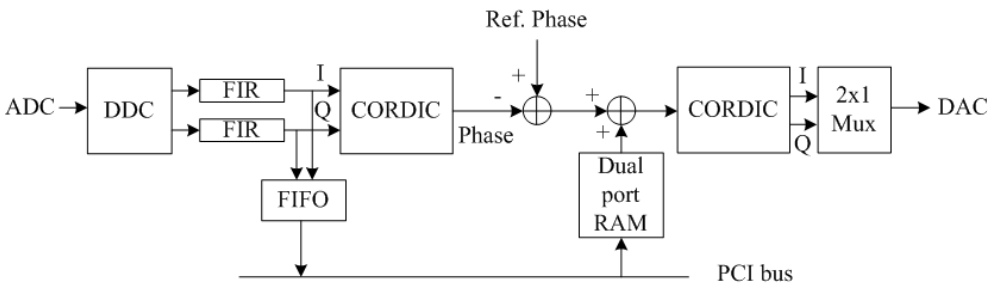

Figure 4: Layout of one channel in FPGA

ADC & DAC

ICS572B uses two 14-bit ADCs (AD6645), which work in simultaneous mode. Data from two ADCs directly send to FPGA. The latency of ADC is four sampling points, about 40ns.

ICS572B uses two 14-bit DACs (AD9857), which contain digital up-converter. DAC is set in quadrature modulation mode, and frequency-tuning value of DDS is set to 1/8. By these proper settings, DAC can up-convert I/Q input data to IF signal (25.6MHz). Because DAC sampling clock is synchronized with reference IF signal, DAC output is also synchronized with reference IF signal. FPGA directly send I/Q data to two DACs simultaneously. The latency of DAC is about 510ns.

SIGNAL PROCESSING & CONTROL

Signal processing in phase control system includes digital I/Q demodulation, digital I/Q modulation, I/Q to phase conversion, phase to I/Q conversion, and FIR filter.

DDC in Fig. 4 is the digital I/Q demodulation. ADC sampling clock is four times of input signal, so digital I/Q can be attained by

$$\begin{cases} I(n) = [x(4n-3) - x(4n-1)]/2 \\ Q(n) = [x(4n) - x(4n-2)]/2 \end{cases} \quad (1)$$

FPGA clock is used to align four successive sampling data to generate a couple of I/Q data.

Two FIR filters are used to compensate phase shift between I/Q caused by digital I/Q demodulation algorithm.

Because the amplitude of power amplifier output signal cannot control by its input signal, the close-loop in phase control system should not contain amplitude data, otherwise the close-loop may be work improperly, so I/Q to phase conversion is used. Compared with look-up-table algorithm, it spends less FPGA resource to implement CORDIC (Coordinated Rotation Digital Computer) algorithm as I/Q to phase conversion or phase to I/Q

conversion [3]. We use 12 taps CORDIC, and the phase conversion accuracy is better than 0.1 degree.

Feed-forward control is also realized in FPGA. The phase difference is attained by comparing reference phase with sampled phase data; the phase of feed-forward control is attained by add phase difference with feed-forward phase vector in dual port RAM.

DAC input data is the interleaved I/Q data. So it is needed to convert the phase of feed-forward control to I/Q data, which is realized by 12 taps CORDIC; also it is needed to convert parallel I/Q data to interleaved data stream, which is realized by 2x1 multiplexer.

The latency of every part in FPGA is listed below:

- DDC: 1 period
- FIR: 1 period
- CORDIC: 3x2 periods
- Feed-forward control: 2 periods
- 2x1 multiplexer: 1 period

So the total delay of phase control system is about 1us (12*40ns + 510ns).

Software

Iterative algorithm calculation for feed-forward control is run under VxWorks operation system. At the end of one pulse, software is triggered by interrupt to read FIFO, which stores all I/Q data in the pulse. Feed-forward phase vector is calculated according with these I/Q data, and then written to dual port RAM in FPGA. After finish data writing, software waits for next interrupt.

PRELIMINARY TEST

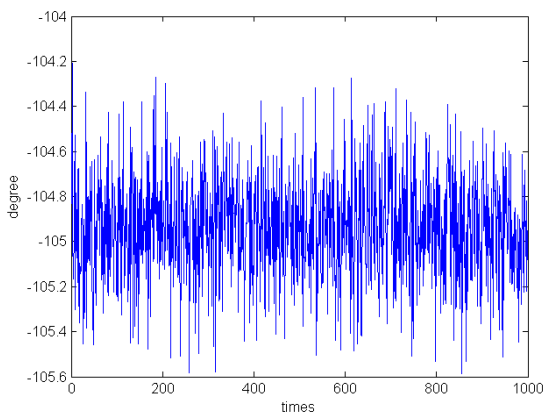

Figure 5: Background noise of phase control system

Firstly, we tested the background noise of phase control system in LINAC operation condition. In the test, RF reference signal is connected both Kly. A port and RF ref. port in RF front-end. The testing data is acquired by measuring one point phase (2us after external trigger rising edge) 1000 times. From the test result, shown in Fig.5, the background phase noise is within ±0.6 degree.

Secondly, we placed digital phase control system in SSRF LIANC and set in open loop mode, then measured interpulse phase 1000 times to attain phase shift of klystron forward signal, shown in Fig. 6. From the testing result, the phase shift of klystron forward signal is more than 10 degree, and digital phase control system is essential to satisfy the requirement of phase stability.

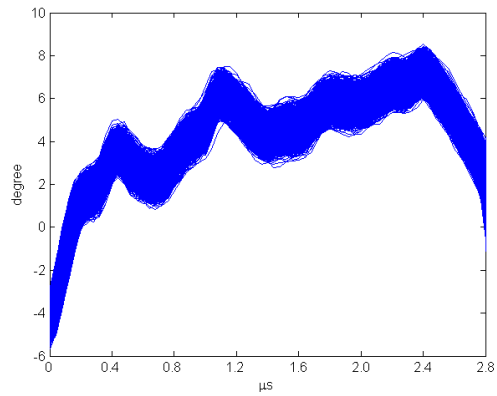

Figure 6: Interpulse phase shift of klystron forward signal

Due to the present commissioning stage for SSRF, there is no enough machine study time in LIANC. So, the close-loop of phase control system will be further tested in future. But the preliminary test result has proved the feasibility of digital phase control system design, and the performance of close-loop could be foreseeable.

Clock management module in phase control system could reduce the complexity of RF signal distribution system, so it is a helpful reference design for next phase control system in FEL.

REFERENCES

[1] SSRF project team, SSRF preliminary design, internal report, Nov. 2004.

[2] Interactive circuits and system Ltd., ICS-572B operating manual, July 2005.

[3] J.E. Volder, The CORDIC trigonometric computing technique. IRE Trans. on Electronic Computer, 1959,8(3): 330-334