APPLICATIONS OF RECONFIGURABLE LOGIC DEVICES FOR ACCELERATOR CONTROLS

T.Fukui, T.Masuda, S.Sasaki, T.Takashima, R.Tanaka
SPring-8, Hyogo, 679-5198, Japan

Abstract

Recently, algorithm reconfigurable devices such as field programmable gate arrays (FPGA) and digital signal processors (DSP) have been widely used in the commercial product as the system-on-chip (SoC) applications. Those devices make it possible to develop a high performance system for a short period of time, and moreover it is possible to make small quantity with reasonable cost. The structure of SoC devices with FPGA is fully flexible and can respond to change of the logic of a control system easily. The capability of modifying the logic enables us to easily implement future additions to the system. At present, we have developed new remote I/O system consisting of VME boards and remote I/O cards with FPGA chips. The VME boards and remote I/O cards are communicating via optical fiber links. The circuits with DSP chips for electron-beam position monitoring are under development for high precision beam orbit measurements of the SPring-8 storage ring. Those applications show a flexible and expandable nature of the reconfigurable logic devices. The SoC system will fit many types of digital signal processing, such as a very high-speed feedback or a timing system in the accelerator control system in the future. We will present some of examples as potential applications in this paper.

INTRODUCTION

More than 20 years ago, most of accelerator control systems consisted of discrete modules and many cables. Cables and connectors ware source of failure points. Some of these modules were replaced by ASIC to reduce cables and connectors. These solutions were very expensive for small quantity and not flexible enough for an accelerator control system. Last decade, the system-on-chip (SoC) applications based on field programmable gate arrays (FPGA) and digital signal processors (DSP) have been used in much area like telecommunication systems. The SoC make it possible to develop a high performance system for a short period of time and flexible to change of the logic. These features of the SoC are suitable for an accelerator control system. We develop several applications using DSP and FPGA because of the flexibility, reliability and short development time.

APPLICATIONS AT THE SPRING-8

The first application is a remote I/O system consisting of VME boards and remote I/O cards with FPGA chips. We have been using three types of remote I/O system for the booster and the storage ring magnet power supply. These are relatively slow, typical response time is an order of msec. On the other hand, there are high-speed optical links, such as Fiber Channel in commercial products but these are expensive and complex. New remote I/O system was designed to be expandable and low cost with order of μsec response. FPGA chips meet this requirement.

The second one is an electron-beam position monitoring system for the SPring-8 storage ring with high performance DSP chips with floating point calculation. The existing system is using an rms-DC conversion with analog circuit. An accuracy of beam position measuring is close to sub-micron with 0.25sec integration time caused by the difficulty to optimise signal to noise ratio. Because a vertical beam size is less than 10μm, sub-micron accuracy is required to achieve the stable beams. The new system could optimise signal to noise ratio by digital signal processing and integration time will be reduced to 1msec.

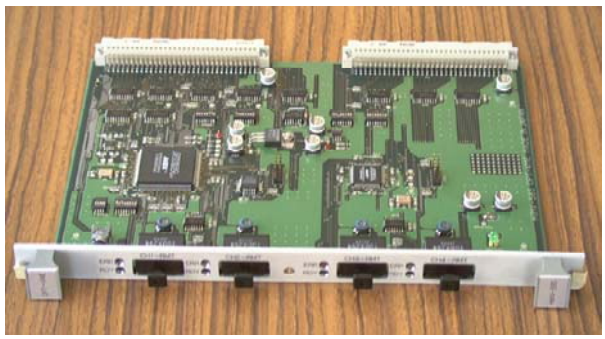

Figure 1: A view of new remote I/O master card.

Remote I/O System

New remote I/O system was developed with two phases. At first, it was developed for beam position monitor (BPM) for a linac of the SPring-8. [1] Requirements of the system are

1. This BPM system needs data every 20μsec to recognize an analog to digital conversion period of BPM signals.
2. The system needs to read large number of the BPMs.
3. The system has to avoid the electro-magnetic noise from modulators of the linac.

All logics of the VME board (as a master) or remote I/O card (as a slave) are in one chip of FPGA including the VME bus I/O as shown in figure 1. This system uses the polymer-clad fiber with 20Mbps link speed. The master card has two modes, a DI and a DO mode. The DI mode receives data from slave cards every 20μsec. The DO mode sends a data to slave cards every 20μsec. The master card has four channels of optical link and each slave card sends or receives four sets of 16bits(data bits)+1bit(strobe bit) data. We call this version OPT-VME1. We use the DI mode for the linac BPM system.

This system was installed in January, 2003, and has been running successfully. Figure 2 shows the electron beam trajectory of the linac with a single shot.

At the second phase, we developed three types of slave cards, based on the successful operation of the OPT-VME1 and the reconfigurable capability of FPGA. We decided to expand the function of this system for the renewal of the linac control system. [2] Each card has functions below

1. DI/O card: four sets of 16bits+1bit digital output and four sets of 16bits+1bit digital input.
   Total is 68bits digital input/output per slave card.
2. AI card: 16 channels of analog input with 16bits resolution.
3. Combo card: two sets of 16bits+1bit digital input/output and two sets of analog input/output with 16bits resolution.

AI cards were used to readout of equipment signals for vacuum systems and wall current monitors. Combo cards were used for magnet power supplies, and each card could control two magnet power supplies. Even if communications between the master card and the slave card are lost, a digital output or an analog output keeps the state. This feature allows us to reboot a CPU on VME without interfering the beam operation.

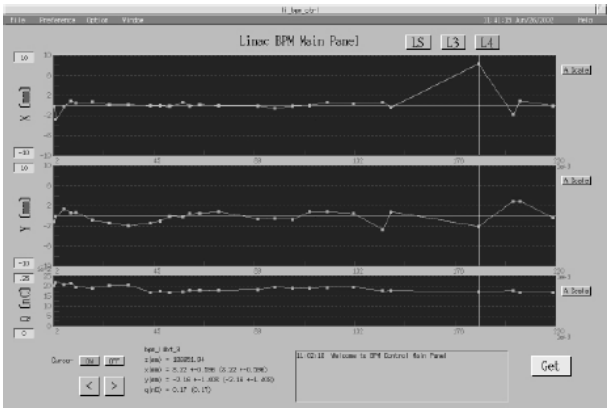

Figure 2: A trajectory measurement of an electron beam at the linac.

In the second phase, we need to change functions of the master card. The DO mode was removed and the DI/O mode was added. The DI/O mode receives or sends data with command. Each function takes 40 μsec because it needs twice of the data size (command and data). Also we added a new function for the AI card. The AI card has four sets of banks and each bank includes four channels of analog input. The master card has a command to switch the bank of the slave card. We call this version OPT-VME2. These changes caused incompatibility with the OPT-VME1. Fortunately, we could use an FPGA with a larger gate size in the same package. This makes us possible to use the same printed circuit board for the mater card. In addition, it is possible to change the OPT-VME1 to the subset of the OPT-VME2. The DI card is also need to change to keep compatibility with the OPT-VME2. At summer 2003, we were renewal of the linac control system with OPT-VME2 and slave card. As a result, total number of CPUs is reduced from 27 to 10, and the VME systems were moved away from klystron modulators.

We already developed a new slave card. It has functions of analog pattern generation with 16bit resolution and a 1M words buffer. This could be used for the corrector magnets of the booster synchrotron. A flexible and expandable nature of FPGA allows us to change a functionality of I/O board without modification of a printed circuit board design.

Electron-beam Position Monitoring System

The new system consists of three parts: an analog signal processing unit, AD unit, and DSP board, as shown in figure 3. One set of analog signal processing unit manages twelve BPMs. The AD unit and the DSP board are connected with optical cables to avoid the effect of digital noise. We adopted a direct sampling demodulation with intermediate frequency (IF) signal, which is the method to sample the IF signal with an ADC and digitally rectify the signal. One of the advantages of the method is that a smaller non-linearity is expected compared with an analog demodulation method.

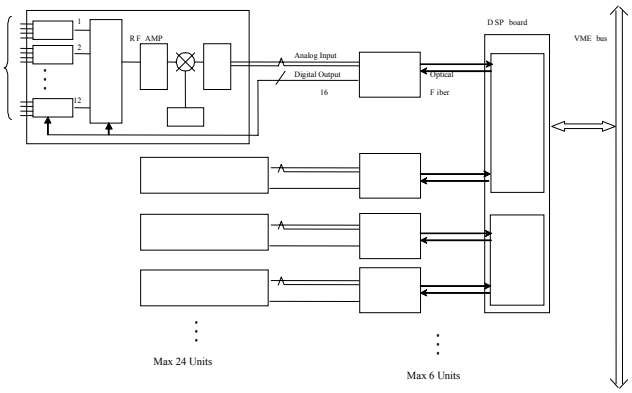

Figure 3: A schematic view of the beam position monitoring system.

A high-resolution ADC with fast sampling rate is necessary for the high-speed and high-resolution digital rectification. And computing power is also required for the DSP. We decided to use a 1MPS, 16bit ADC (Analog Devices AD7677) for the AD conversion, and the DSP (TMS320C6713) to perform the digital demodulation. The DSP board is designed as a VME board and easily fits to a possible change of the processing algorithm. The FPGAs are used for interfacing the TAXI chips to the ADC and DSP, as shown in figure 4. These parts are subjected to a less frequent change of the procedure of interface. A control code for the DSP can be loaded by two methods. One method uses an on-board EPROM. The other is loading the code from VME CPU board via VME bus. The latter is called “host boot”. Actual processing is as follows; IF frequency 250kHz sinusoidal wave signal is sampled at 1 MSPS rate. It means the $0, \pi/2, \pi, 3/2\,\pi$ phase sampling. An amplitude is calculated from the sampled data by IQ detection with1000-samplings for

each electrode. Using 4 amplitude data corresponding to four pickup buttons for each BPM, a position is calculated with the position sensitivity coefficients. Total processing time of 12 BPMs was measured to be 49 msec including one msec overhead. Most of the overhead comes from interfacing with TAXI chips. Actual calculation time is 57μsec for the amplitudes, and 15μsec for the position calculation, with the optimisation by the complier. The time for calculation becomes much longer without the optimisation. Considering the processing time, a more complex calculation, such as FFT, is possible within a reasonable period of time. The target plan for installing the system to the SPring-8 storage ring is the installation during the summer shutdown in the year 2005.

We expect that the system is applicable to a global fast feed back also. Processing period required by the global feedback is less than one ms. It is possible to fit the requirement using the same DSP board, by reconfiguring the logic.

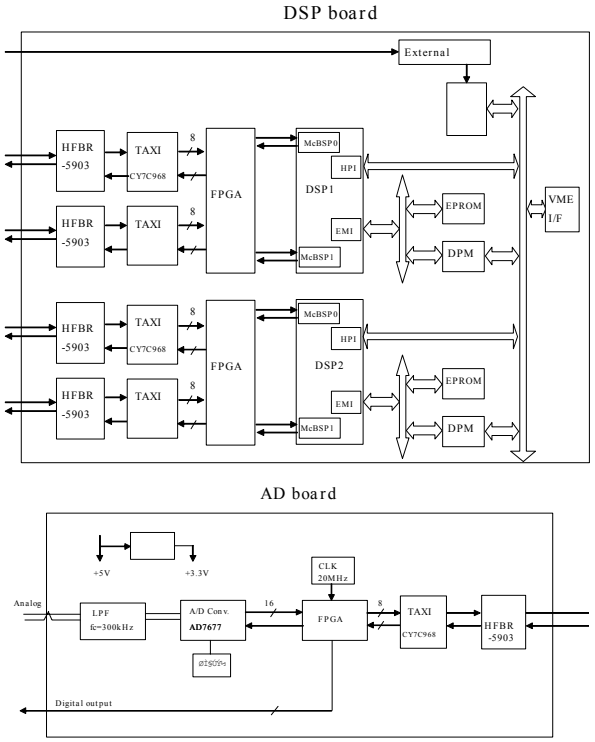

Figure 4: A block diagram of the DSP board and AD board.

Other Applications

A CPLD-base timing system was developed for the SPring-8 accelerator complex [3]. A CPLD was used for only logic part and timing generation was made by discrete logic. A jitter less than 10ps is required for the timing system. FPGA or CPLD is not available to achieve this requirement at commercial base. It may be possible to achieve the requirement by 10 Gigabit Ethernet technologies in near future. If it is available we could replace many discrete modules to single FPGA.

One more application is bunch-by-bunch feedback of the transverse beam motion. The SPring-8 storage ring is operated with RF frequency of 508.58MHz. Six FPGA modules detect beam motions and one FPGA serialize these data to 1Gs/sec DA converter for vertical and horizontal axis. Detection modules are running at 85MHz as time division multiplexing. The serializer module is running at 254MHz with double edge data output. This system was installed on the SPring-8 in summer 2003. It will be possible to make one chip for detection module and serialize module by using high performance and large gate size FPGA.

SUMMARY

We have developed a new remote I/O system consisting of VME boards and slave I/O cards with single FPGA chip as the SoC application. This system is used for the SPring-8 linac control system and operated successfully. Also we added several functions and develop new slave board. The structure of the SoC devices with FPGA is fully flexible and can respond to change of the logic of the control system easily. The VME boards with DSP chips for electron-beam position monitoring are under development for high precision beam orbit measurements of the SPring-8 storage ring. A preliminary result shows a good performance of a processing capability. The algorithm reconfigurable devices make development of a high performance system possible for a short period. Those applications show the flexible and expandable nature of the reconfigurable logic devices. The SoC system will fit many types of digital signal processing, such as a very high-speed feedback or a timing system in the future accelerator control system.

REFERENCES

[1] K.Yanagida et. al., “Commissioning of The SPring-8 Linac BPM System.” Linac2002, Gyeongju, August 2002.

[2] T.Masuda et. al., “Upgrade of the SPring-8 Linac Control by Re-engineering the VME Systems for Maximizing Availability,” Icalepcs2003, Gyeongju, October 2003.

[3] N.Hosoda et. al., “Reconfigurable Timing Controller using PLDs,” Icalepcs2003, Gyeongju, October 2003