The RF System of the HIMAC Synchrotron

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Abstract

An RF system of the HIMAC synchrotron has been constructed. In the control system we have adopted a digital feed back circuit with a digital synthesizer (DS). This paper describes the RF system and its tested results.

1. Introduction

HIMAC is a heavy ion accelerator facility dedicated to the medical use, especially for the clinical treatment of tumors. In table 1 major parameters of the HIMAC synchrotron are listed. The characteristic requirements for the RF acceleration system (Fig.1) of this synchrotron are the following.
1) Wide RF range (from 1MHz to 8MHz).
2) Acceleration voltage of more than 6kV with one cavity.
3) Wide beam intensity range between 10^7ppp and 10^{11}ppp in the synchrotron.

To control wide acceleration frequency stably with low FM noise, a digital control system with a digital synthesizer (Stanford Telecommunication, STEL-1375a) has been adopted for the RF control system. Beam monitors of position (ΔR) and phase ($\Delta\phi$), which can be used with wide beam intensity range, have been developed. This $\Delta\phi$ monitor must have fast response to use for the feedback loop which must damp the synchrotron oscillation. We have checked this feedback loop with the developed simulator circuit in a fac

tory. Also the beam acceleration test with this control system has been performed at TARN-II in INS (Institute for Nuclear Study, University of Tokyo).

Table 1
Parameters of the HIMAC synchrotron

Beam species	He^{2+} to Ar^{18+}
Injection energy	6 MeV/u
Momentum spread of the injected beam	$<\pm 0.3\%$
B (injection/maximum)	.1/1.5 T
Field ramp	2 T/sec
Maximum beam energy	800MeV/u
Beam intensity range	10^7 ppp -10^{11} ppp
Circumference	129.6 m
Transition γ	3.67
Harmonic number	4
Frequency range	1 - 8 MHz
Filling factor	0.8
Peak voltage	<11 kV (at 1MHz)
Synchrotron frequency	1 - 4 kHz

2. RF Cavity

The RF cavity has a single gap and two ferrite loaded quarter wave coaxial resonators. This cavity has almost same design as that of TARN-II at INS.[1] A resonance frequency is changed by factor 8 with current on a ferrite bias winding.
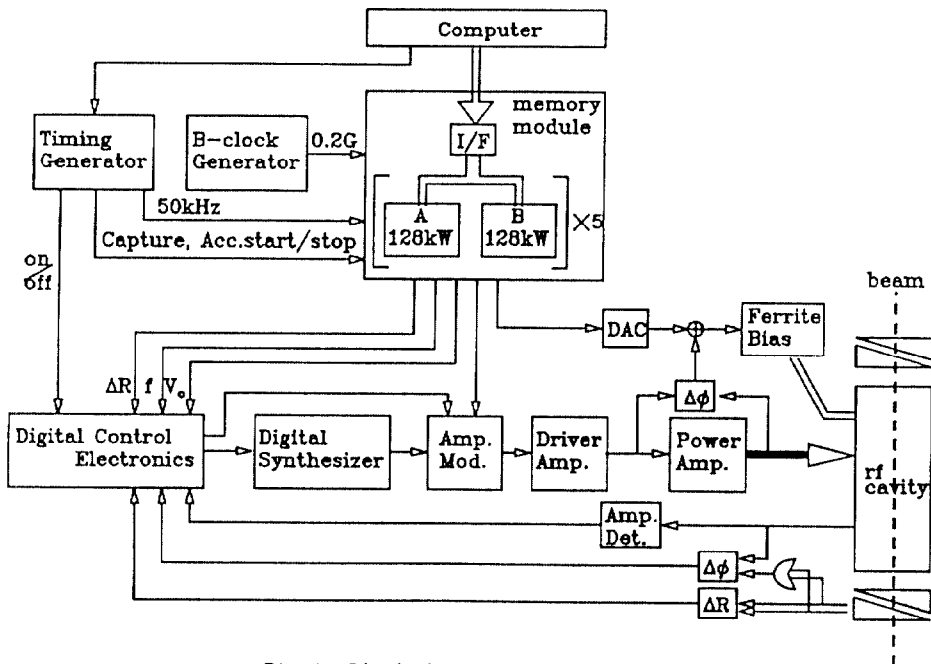

Fig.1. Block diagram of the RF system

RF high power source consists of a transistor 500 W driver amplifier (ENI A500) and a final tetrode amplifier (Eimac 4CW100000E). These amplifiers are wide band frequency type, and all pass network is adopted at the input circuit of the final amplifier.

Ferrite bias power supply is operated by the pattern function of the pattern memory and correction function from $\Delta\phi$(Vc-Vg) signal. It is a transistor dropper power supply whose maximum output current is 900 A, and unity gain bandwidth is about 4 kHz. The load inductance changed widely from 16 μH to 1 mH. Therefore a current feedback gain is variable as a function of output current.

3. Pattern memory

The pattern memory devices are designed to generate the patterns of an accelerating frequency, an accelerating voltage, a ferrite bias current, a bias of beam position, and an accelerating voltage correction. In the computer of man-machine interface, data points of the patterns are given by the formula firstly and can be corrected later by the operator. These pattern data are sent to the computer (RF computer) which controls acceleration system directly. The data size of one pattern must be less than 128k words. For each kind of pattern there are two memory units. One memory unit is used to control each device, and the another is used to change the pattern data in it. With these two memories the pattern data can be changed without stop of the system. This makes system tuning easy.

To output the pattern data from the memory to the control devices, two kinds of pulses are used to drive the pointer address. One is clock pulse of 50 kHz (T-clock) and the another is the pulse of increment (or decrement) of the dipole magnetic field (B-clock). One pulse of the B$^+$-clock (B$^-$-clock) corresponds to 0.2 Gauss increment (decrement). To generate the pattern data with these clocks, pattern memories are divided into following three regions.

1) region-1
   T-clock is used to generate the pattern data, which determine the pattern in the flat base.
2) region-2
   B-clock is used to generate the pattern of the accelerating period.
3) region-3
   T-clock is used again to generate the pattern in the flat top.

An event pulse of the beam capture starts to advance the pattern memory address of region-1 with T-clock. To start the beam acceleration, an event pulse changes the T-clock to B-clock and jumps to the memory address in region-2 where the output frequency data are the same as the last data. In the flat top, an event pulse changes the memory address to the first address of the region-3. If there is difference between the last output data and the data of the head address in region-3, the output value is moved to the data of the head address with one bit step. This function make the change of the output value smooth and is important not to loss the beam.

4. Beam monitors

4.1. Pick-up electrode

A monitor electrode consists of four diagonally cut copper plates which are insulated by ceramic blocks from ground plates. Two plates are for right signal(R) and the other two plates are for left signal(L). Each pairs of these plates are connected in the vacuum chamber to make the right and left beam signals. There are no side plates to diminish the noise due to the beam hitting. The aperture of the monitor is 192 mm wide and 56 mm high, and its length is 250 mm. The gap between pick-up electrode and ground plate is 5 mm to make the capacitance of the plate 200 pF. Two identical monitor units of are symmetrically installed at both sides of the rf cavity, and the each L and R signals from the monitors are then combined to produce the final L and R signals. This summation is expected to reduce the rf noise, because two rf noises have opposite phase.

4.2. Electronics

The first amplifier is directly connected to each electrode and have 100 kΩ input impedance. The thermal noise voltage from this resistor is calculated with following formula;

$$V = 4\ kT\Delta f\ \frac{R}{1 + (2\pi fCR)^2} \qquad (1)$$

here k = 1.38 x 10^{-23} (J/K), T is temperature (K), f and Δf are observing frequency and its band width, C is capacitance of the pick-up electrode, and R is input resistance. With above formula the noise voltage at 1 and 8 MHz are 0.6 and 0.08 nV/$\sqrt{}$Hz, respectively. These values are small compared with FET noise voltage of 1.2 nV/$\sqrt{}$Hz. An output impedance of the amplifier is 50 Ω and gains of -10 dB or 20 dB can be selected. The second amplifier has gains of 0dB or 40 dB. The beam signal is further amplified by a double heterodyne module whose gain is between 0 dB and 50 dB with 10 dB step. Selecting the combination of the gain values in each amplifier, total gain range of the monitor system is from 0 dB to 100 dB with 10 dB step.

In this heterodyne module the fundamental frequency of beam signal is converted to fixed frequency of 50 MHz firstly. This frequency conversion is done with a double balanced mixer (DBM) following a bandpass filter(BPF) with bandwidth of 160 kHz, which is wide enough to use for the $\Delta\phi$ feedback loop. In the second stage the frequency is converted to 455 kHz with DBM and the low pass filter (LPF) of 1 MHz is used.

In a processor for ΔR detection, we have used amplitude to phase conversion and obtain the following output.

$$2.5\ \sin\ [2\ \arctan\ \{(R -L) / (R + L) \}]\ (V) \qquad (2)$$

For the $\Delta\phi$ detection the R and L signals are added to make the beam signal (R + L). In the $\Delta\phi$ processor a digital phase meter with a band rejection filter at 455 kHz and a low pass filter of 330 kHz are used. The errors of the $\Delta\phi$ and ΔR at the gain setting of 70 dB are ± 3° and ± 2.5 mm, respectively. This gain corresponds to rf signal amplitude of 25 μV (o-p) and minimum beam intensity of 10^7 ppp (He^{2+}) in HIMAC.

The responses of both monitors are fast enough to be used for the feed back loops. The response delay of $\Delta\phi$ and ΔR monitors for step function are 7 μs and 20 μs, respectively.

5. Digital control circuit

To control the wide range accelerating frequency stably, we have adopted the digital control circuit. The ΔR and $\Delta\phi$ analog signals are converted to digi-

tal data every 2μs with eleven bit (+ sign bit) ADCs which are located near the rf cavity together with the beam monitor electronics. One bit corresponds to 2.4mV (0.052mm in the ΔR monitor and 0.087° in the $\Delta\phi$ monitor). In the control module, the ΔR digital datum is biased firstly to control the beam center at optimum position. Then the start-stop function of the feed back with time constant of about 100μs are followed. The both data are added after adjustments of a proportional loop gain in the $\Delta\phi$ feed back, and proportional and integral loop gains in the ΔR feed back. This sum datum is further added to the frequency pattern data from the memory module. The datum of twenty bits is used to drive the DS, and one bit corresponds to 10Hz. Clock frequency of 10MHz is used for the digital processing, and the time delay between digitizing the analog data (ΔR and $\Delta\phi$) and driving the DS with new datum is 2μs.

6. Test of the system

To make sure the performance of the rf system, the high power and control system have been combined and tested at Toshiba Fuchu works. After tuning the system, we could sweep the cavity frequency from 1 MHz to 8 MHz in 0.7 second with the acceleration voltage of 6kV. In the test we have also measured the dependence of Q-value on the rf amplitude. There is strong dependence at low frequency. Since the rf amplitude dependence of permeability in th case of TDK-SY6 is small, the shunt impedance R at Vc = 6 kV is evaluated as follows;

$$R = (QRo)/Qo, \tag{3}$$

where Ro and Qo are measured values at low power. The shunt impedance R is nearly constant from 1 MHz to 8 MHz at an acceleration voltage of 6 kV.

After the high power test the cavity has been checked, and a damage of the capacitor which is attached to a ferrite bias winding was found. This break is due to two small parasitic resonances which were not found at low power test with zero ferrite bias current. The frequencies of these resonances were 2.3 MHz and 4.3 MHz.

To test the $\Delta\phi$ feed back loop, we have used a newly developed simulator which is a circuit to generate the synchrotron like oscillation. It has the similar transfer function as the synchrotron oscillation. The test was performed under the condition that f_{rf}=1 MHz and f_s (frequency of the synchrotron oscillation) = 4, 6, and 7kHz. In the test, the feed back loop could damp the oscillation of 6kHz quickly. From these results, it is clear that the $\Delta\phi$ feed back loop has fast response which is good enough for our purpose, because the maximum frequency of the synchrotron oscillation is 4 kHz in HIMAC synchrotron.

7. Beam test of the control system

If there is a large phase jump when the accelerating frequency is swept, the accelerated beam will be lost. To make sure that there is no large phase jump in our DS, we have performed the beam test at TARN-II. In the beam test, we have joined our RF control system (computer, timing generator, memory module, digital low level electronics, digital synthesizer, beam monitor electronics) with the RF system of TARN-II[1],[2]. Though the beam intensity was very low (8 × 10^6 ppp), we could accelerate the He^{2+} beam from 10MeV/u to 160MeV/u. These energies correspond to the acceleration frequencies of 1.1 MHz and 4.0 MHz.

respectively. The tuning of the control system was very simple and easy to succeed in the beam acceleration. This is the characteristic feature of the digital control system and important in the medical accelerator. The acceleration efficiency was about 55%. The possible reasons of the beam loss are;

1) Large white noise in the beam monitors.
2) The RF noise whose effect was enlarged by the low beam intensity.
3) The B-clock step of 1 Gauss which produces the longitudinal beam emittance growth. (In the analog system, we can use the filter to smooth this B-clock step.)

Improving signal to noise ratio with the longer beam monitor electrode and generating small step function of frequency with the B-clock step of 0.2 Gauss in the HIMAC RF system, it will be possible to accelerate the beam without large beam loss.

8. Summary

We have constructed the acceleration system for the HIMAC synchrotron. In the high power test, the rf frequency could be swept from 1 to 8 MHz with 6 kV. Further increase of the voltage is left. The beam monitor with good S/N ratio in low beam intensity have been developed. For the ΔR and $\Delta\phi$ feed back system, digital control circuit with DS were developed. The beam test of the control system has been performed, and we could accelerate the beam with very low intensity, which corresponds to minimum beam intensity in the HIMAC synchrotron.

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10. References

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