ADVANCED CONCEPTS IN ACCELERATOR TIMING CONTROL*

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The control system for the Booster accelerator presently under construction at BNL includes a timing section with serial high speed coded data distribution, computer based encoders for both real time and field driven clocks and a method of easily tracking the performance and reliability of these timing streams. We have developed a simple method for the generation of timing which operates to produce pulses which may be repeated as desired with minimal latency.

The operative approach is to treat the Booster as one among several accelerators in the AGS complex which interact to fill the need of a combined physics program, but which also may have physics needs of their own. These machines are the TVDG, LINAC, BOOSTER & AGS. This concept is extendable to encompass our future needs including RHIC operation. Our system supports limited pulse to pulse modulation via a master timer or "super cycle generator" (SCG). Our intent is to have some number of flexible cycle options, but not to solve the general case. The SCG is line synched to help with the second order power line dependent effects we have already observed between the AGS and the LINAC. The resolution offered in the SCG of 1/60 second is deemed adequate for our needs.

A major issue was the use of absolute or delta value setpoints. In an "absolute" system every timer within the Booster would pulse at an absolute count from the cycle start event. In a "delta" system timers and their setpoints are cascaded. We choose to have a basically "absolute" system with as many events timed from a single start pulse as possible. Delta mode modules are provided for use as needed. We claim that a mainly "absolute" system is easier to validate.

At the accelerator level, that is within the scope of the Booster Timing Generator (BTG), the new timing system can be thought of as a Real Time (RT) section consisting of 2,000 channels of Autodets (computer controlled predetermined counters) each running on a common 1 Mhz clock and a Gauss section with an additional 2,000 channels of Autodets running on a gauss clock with a resolution of .1 gauss. The RT and Gauss sections use memory generated timing pulses. The BTG distributes RT and Gauss Clock Codes in the form of two separate encoded streams. Credit for the concept of serial encoded data streams as distributors of accelerator timing signals goes to Robert Ducar of FermiLab (ref 1).

Included are some 100 channels of conventional Autocets (computer loaded count down timers with individual clock, start and output pulse lines). These are added to support applications which cannot be efficiently handled by the new approach: applications which require field determined events generated after a given time related signal, those which require field derived events to then trigger a time synchronized event, events needed at the RF frequency rate, timing pulses for those systems which cannot support the indeterminacy of encoded event signals.

The SCG indicates to the BTG which user cycle to run next and when to start the new cycle. The SCG produces among other pulses a Booster arming or pre-pulse signal and a Booster start of cycle signal. The nominal rep rate of the SCG is adjustadjustable from 33ms to 72 hours. During this super cycle up to 255 action codes can be repeated with a resolution of 1/60 sec as often as necessary.

The RT and Gauss clocks operate as follows: computer generated codes and/or pulse generated signals are turned into encoded timing streams by an event encoder. There are 30 pulse generated and one computer input channel to the event encoder. Each pulse input channel is assigned an 8 bit code. The computer input is already coded. When an event input is triggered, it's code is generated, encoded onto a clock train and transmitted in a serial format on a single cable or fiber optic trunk. Typical resolution of event timers is 1.2uS. The input channels to the event encoder are ordered and thus it is possible for a higher priority event bump (delay) a lower priority event.

Encoded and memory driven channels are powerful, but are deficient compared to older designs for some applications. The new units are each run from a single clock (one unit from time and another unit with a field clock) and thus are not cascadable. Counters are long, allowing operation over a cycle of 16 seconds (or 1.6×10^6 gauss ticks) with a resolution of 1 microseconds (.1 gauss ticks). Our inability to cascade is mitigated by the computer's ability to define groups of timing setpoints and by the units capability for fine resolution over the full cycle range. A new capability, multiple pulsing of channel (multiple use of the same code) is supported at the cost of using up one of the available two thousand channels for each output. Another disadvantage is the new system's inability to generate more than one output pulse at exactly the same time instant. The new system provides pulses which under contention may be delayed from the desired time because of priority circuits and encoding delays.

We have not yet decided whether to deploy coaxial cables or to distribute these encoded signals as part of a fiber optic back bone which will also carry other control related information. The Decoder Modules used will be based on the LSI decoder designed by FermiLab; they demodulate the code stream and decode it into pulses.

For ease of use and debugging, a Line Moniter will be provided as a part of the Timing Distribution System. Its function is to record the codes that

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are transmitted on the encoded trunks and enable a comparison between the expected codes and the received codes, or the previous cycle with the current cycle.

The output signal from any part of the BTG may be used to arm or fire any other part; e.g. field event trigger is patched to RT and is included for distribution. These connections will be made with a physical rather than software patch.

When timing signals are received by the devices they are decoded into a 10MHz clock and a 8 bit event code. The event code is further decoded to pulses. Parity on the incoming transmission is checked as a means of transmission error detection.

The Booster operates to provide the AGS with four proton beam bunches per AGS cycle. Thus for each AGS cycle that occurs, four Booster cycle events are needed. The BTG would then provide the Booster with four separate pulses with each one starting it's own Booster cycle. Since the cycle time of the Booster is 133mS, that of the Linac is 100mS and for the purposes of this example that of the AGS is nominally 2000mS then the SCG would be adjusted to have a repeating pattern of some 120 ticks; these signals are 60Hz power line locked.

If heavy ions are used then the above scenario is essentially the same except that the LINAC could run free at its maximum rate with timing generated by the SCG. The TVDG and the Booster rep rate for heavy ions will be 1Hz. Thus all machines in the system are ultimately synchronized to the AGS by the SCG and in some future scenario to RHIC.

The SCG is a real time event encoder. It outputs codes at scheduled event times. The codes tell the generators to preload or start a user cycle; the codes tell the generators what user cycle is next and when to start the new cycle. The SCG repeats the supercycle: A supercycle can last from 2 clocks (33mS) to 16M clocks (73 hrs). During each supercycle, codes can be scheduled for output at up to 4000 event times. Up to five codes can be output for each event. This allows a seperate code for each timing generator to be outputed on the same supercycle clock tick.

The accelerator control system employs a distributed, hierarchical computer system; its lowest layer is the device controller. The SCG and BTG are connected to the computer network as device controllers.

The supercycle may be modified over the network. Once a new table of event times and output codes has been generated, the next supercycle that starts will run the modified supercycle. Since the codes are output serially, there will be a delay between the first and last codes. There are 255 supercycle codes. Several user cycle preload codes and one start cycle code are assigned to each timing generated. The pre-load codes will be used by the timing generator to choose one of several stored cycle definition tables to be loaded into each of the local clock generator boards and are ready to run when the start cycle code is received. If no new cycle has been loaded, the previous cycle will repeat.

The SCG will interface to the computer network as a Device Controller. The supercycle may be modified by transmitting the changes from the Station over the network. Once the new table of event times and output codes has been generated, the next super cycle that starts will run the modified supercycle. This code is the same as the code used for all other encoded streams used used by the system. It encodes a 10 MHz clock with the serial data. Each code takes 1.2 uS to transmit. Since the codes are output serially, there will be a delay between the first and last codes. There are 255 supercycle codes. The codes will be assigned to each of the accelerator timing generators. Several user cycle preload codes and one start cycle code are assigned to each timing generator. The preload codes will be used by the timing generator to choose one of several stored cycle definition tables to be loaded into each of the local clock generator boards and ready to run when the start cycle code is received. In response to the start cycle code, the loaded cycle will begin. If no new cycle has been loaded, the previous cycle will repeat.

The SCG processor and memory are standard, multibus boards. When a change is made, the update is done in memory and then the updated table is transferred to a clock generated board. Cycle definition tables are time ordered in a special format.

The BTG outputs a Real Time (RT) Code Stream, a Gauss Code Stream and RF Clock Pulses. The RT and Gauss Code Streams are serial outputs in the same form as the SCG Code Stream. A total of 255 separate 8 bit codes may be output on these lines.

The BTG stores and modifies cycle definition tables according to the information transferred over the network. In response to the supercycle preload codes, the correct tables and start addresses are transmitted to the clock boards. Five code tables may be stored in memory for each clock board, enabling five user cycles to be run during a single Supercycle. Formatting of the tables is done by the processor both on initial loading as well as after modifications.

A real time Clock generates the RT Code Stream. It uses our special purpose Clock Generator Board but the count direction is always up. As well as 224 clock generated codes, the RT Clock has 31 cascade inputs which generate codes on the RT Code Stream. When a scheduled time in the cycle definition table is reached, any code stored in the table for that time is outputed. The Gauss Clock uses the same Clock Generator board as the Real Time Clocks. In this case the clock source is the Gauss up/down clock. The cycle definition table in RAM is referenced in both the up and down directions by incrementing or decrementing the Memory Address Register (MAR) depending on the clock direction.

When a scheduled output gauss level is reached, from either direction, the codes in the table are output on the Gauss Code Stream.

A Control block sequences the incrementing and decrementing of the Counter and the Memory Address Register (MAR) and the enabling of the Dual Port RAM and Comparator outputs. It contains status and control registers that are accessible to the multibus. One control bit indicates which if the two buffers to use on the next cycle. The MAR is loaded when next cycle is started. This block also controls clearing of the Counter at cycle start. At the start of a cycle the address of the new

table is loaded into the RAM and the counter is cleared. When the comparator finds the same time in the counter and the table in RAM, the code for that time is converted to an encoded stream and transmitted by the output section.

The RAM will be built with either dual port RAM chips or fast static RAM and logic. The RAM is arranged at 8K x 16 bits on the bus side and 2K x 32 bits on the board side. This is so that the time and the output code are read at once.

The RAM can store two arrays of 2K events. One array is the cycle definition table currently being output and the second array is the cycle definition table for the preloaded cycle.

The (MARs) are two eleven bit Up/Down counters that address the Dual Port RAM. They point to the cycle definition table entries that are currently being looked for. One of the MAR's contains the entry with which a match may occur if the Counter is being incremented. The second MAR points to an address one lower in the RAM. If the Counter is being decremented this MAR is used to address RAM and read the entry to be used by the Comparator. After a match between the RAM and the Counter the MAR's are incremented or decremented by the Control block and the next match is looked for.

The Counter is a 24 bit Up/Down counter. When the Clock Generator is used to generate Real Time codes, the count value represents the time elapsed since the beginning of the cycle. In the case of the Gauss Clock the counter contains the current field level. The up/down feature of the counter is only used by the Gauss clock. A Comparator does a 24 bit compare between the time or field code being read from the RAM and the Counter. Its output is enabled by the Control block after the RAM and Counter inputs are steady. When there is a compare the output codes in the RAM are latched into the Output Control section and output serially. The compare is also input to the Control block so that it can increment the MAR's.

The Priority Encoder latches inputs events and then selects one at a time in priority order. The chosen line is converted into an 8 bit code.

The Output Control block sends the correct code to the Manchester Encoder when there is an event selected by the Priority Encoder. When there is a compare, the code in the table is latched and the clock event line to the Priority Encoder is made active. When the Priority Encoder selects the clock event, a code is output serially by the Manchester Encoder which converts that code into a serial stream.

The Timing Distribution System will provide for long distance information transmission and include a quantity of decoder modules used to demodulate and decode the serial data stream. The module will allow decoding blocks of 8 codes into pules. The decoder will also seperate the 10MHz clock that is encoded with the data. Two clock outputs will be available from the module. They will be strap selectable between 10 MHz, 1 MHz, 100 KHz, 10 KHz and 1 KHz.

The RF Clock Pulses are configured by the cycle definition, but are triggered by pulse inputs. The five clock cards house a total of 100 channels. Each channel supports a separate clock and-start count input; the outputs are not encoded, because this timing is too critical to allow serial codes. The maximum frequency supported is 6 Mhz in order to support RF and Beam timing signals armed by the other generators and clocked by RF zero crossing, phase comparator and beam orbits.

ref 1 Tevatron Serial Data Repeater System, Robert Ducar FERMI National Accelerator Laboratory Batavia, Illinois.