NEW GENERATION OF AD-MEASUREMENT CARDS FOR HIGH ACCURACY MEASUREMENTS

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Abstract

Current transducers are, together with the AD conversion of the current signal, the key elements of high precision power supplies. The accuracy of commercially available current transducers is within the range of a few pp m. Any degradation of this precision by the succeeding stages must be kept as small as possible. Therefore, the accuracy of the AD conversion has to be at least in the same order of magnitude.

Under stable conditions, the accuracy can be improved by measuring and correcting the miscellaneous errors of the ADC and the involved components, such as voltage reference, antialiasing filter and input amplifier. From the measured deviation data a correction look-up table can be derived and later processed.

Further provisions like temperature stabilization, galvanic isolation, electromagnetic shielding, fully differential signal paths and generally a low-noise design allow for further improvements in respect to stability and accuracy.

INTRODUCTION

History and Motivation

Starting in 1999, a large number of fully digitally controlled magnet power supplies are in operation at the Swiss Light Source (SLS) of the Paul Scherrer Institute (PSI) [1], [2]. Since then, this new technology has been increasingly used in other PSI accelerators and different light sources worldwide. Accelerators of the new generation require a very high beam quality and consequentially make high demands on resolution, stability and bandwidth of the magnet power supplies.

As the controller technology used in the SLS is nearly 10 years old, the development of a second generation was started. The new analog-to-digital converter card aims to achieve significant improvement in accuracy at a high data acquisition rate.

What Makes an ADC Un(Precise)?

There are many effects that lead to a non-ideal behavior of an ADC. The main physical effects are:

- Temperature drift of the electronic circuits
- Drift of the characteristics in the course of time (long-term drifts)
- Noise (induced by the circuit itself or by external interferences)
- Offset error
- Gain error
- Integral Nonlinearity (INL) (INL error tells how far away from the ideal transfer function value the measured converter result is).
- Differential Nonlinearity (DNL), DNL reveals how far a code is from a neighboring code.

DESIGN OF THE ADC CARD

Fig. 1 shows a simplified block diagram of the ADC card.

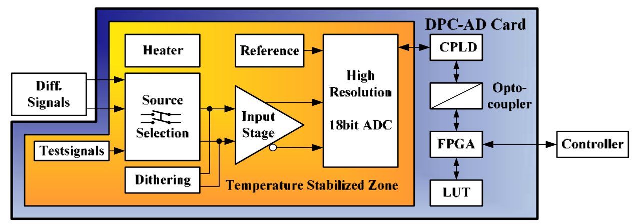

Figure 1: Blockdiagram DPC-AD Card.

The ADC is the key element of any analog-to-digital conversion. We have chosen the ADC AD7634BSTZ from Analog Devices with SAR (successive approximation register) technology and a resolution of 18bit (Sigma-Delta-Converters offer much higher resolution but poor DC characteristics and a fairly high latency). The SAR type is a good compromise between resolution and conversion speed. For power supply applications the latency determines the overall bandwidth and must therefore be as short as possible. Furthermore the selected ADC offers a input voltage range (+/-10V), which is a perfect match with the commonly used output stages of commercially available current transducers.

The analog input stage contains the antialiasing filter. A differential amplifier/driver provides an optimal operation with single as well as differential ended current transducers. Special care had to be taken of the ADC input current spikes due to internal capacitor switching. For self-calibration purposes test signals can be routed to the ADC via a source selection switch array. This feature allows a periodical self calibration of the offset- and gain-error.

The sensitive analog circuit including the ADC is placed on a temperature stabilized zone (TSZ), in order to eliminate temperature drift effects. The circuit is heated and thermally insulated, which allows a constant temperature of 62°C +/-1°C over the whole operating temperature range of 15…45°C.

Special care was taken of the auxiliary supply of the isolated analog circuit. A galvanically isolated zero current switch power converter with a low noise level is implemented.

The quantized output of the ADC is transferred to a CPLD (Complex Programmable Logic Device). There is a dithering function [4] implemented on the CPLD (refer to fig. 2). A pseudo random dithering signal is generated and added to the process signal via a DAC (Digital to Analog Converter). After the conversion, the same dithering signal is subtracted from quantized signal again. Promised by the theory [4] and approved by practical investigations [5], this method reduces the DNL of the ADC. Additional control functions for the ADC are implemented on the same CPLD.

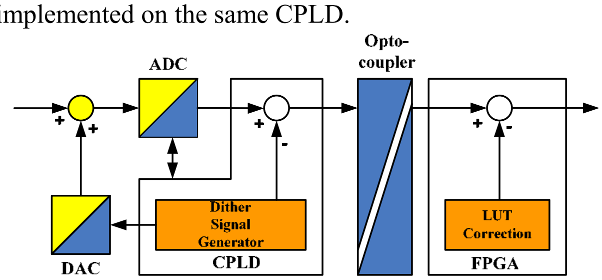

Figure 2: Dithering.

Finally the code words of the ADC are transferred to a FPGA (Field Programmable Gate Array) via optocouplers, which separate the analog and digital part of the circuit. The FPGA handles the error correction, stored in a lookup table (LUT), and the communication with the controller card.

If all the non-ideal behaviours of the ADC, including its surrounding circuits, are known and stable, a correction signal can be determined and added to the quantized signal. An analysing and calibrating system has been developed in order to study the behaviour, measure the errors and compute an error correction function (refer to fig. 3 and [3]).

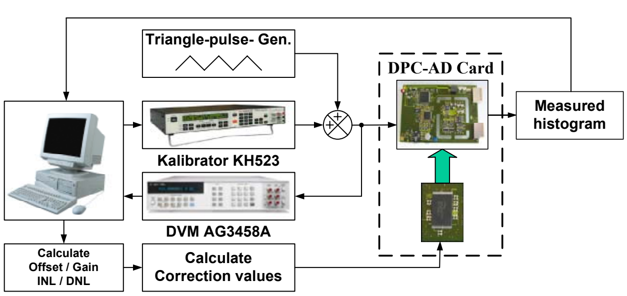

Figure 3: Calibration System.

The accuracy of the AD analyzer and calibrator (fig. 3) is given by the high precision DVM HP3458A which is well established as a reference for high precision measurements. The proposed test uses small triangular stimulus signals superposed on a DC offset value produced by a precise and stable DC-calibrator. The AD converter under test converts this voltage into an equivalent digital code. A Matlab based control system was designed for the data acquisition and analysis. By successive increasing of the DC offset voltage the full ADC range can be processed. The numbers of occurrences of the converted output codes are accumulated in a histogram. (Fig. 4 illustrates this principal for a 3bit ADC).

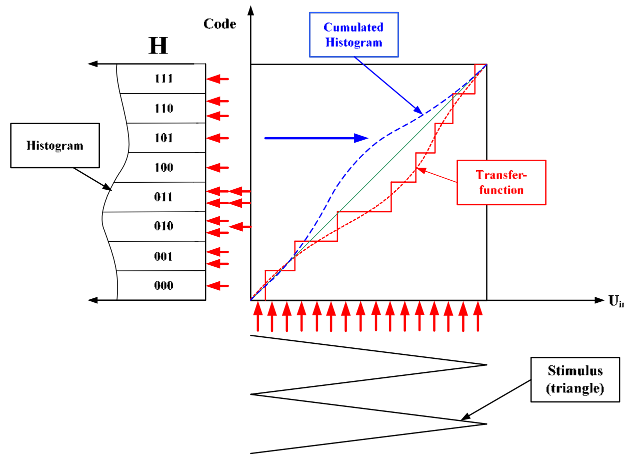

Figure 4: Histogram Method (principal).

From this, a cumulative histogram that counts up the several histogram samples is finally derived. This contains information of all code transition levels and hence the differential and integral nonlinearity DNL/INL. A correction function based on these parameters is computed and stored in a lookup table (LUT) on the ADC board. The converted analog signals are corrected by this LUT into very accurate digital equivalents. As a first order correction the ADC parameters offset and gain can be derived from the first and last transition levels or by linear least-squares estimation techniques. With these two values a simple gain and offset correction can be made.

RESULTS

First prototypes of the high precision ADC measurement card have been built up and analyzed. The temperature stabilization works correct over the temperature range 15…45°C. But, after power-on the circuits need approx. 3 hours to fully stabilize.

The long-term error behaviour of the AD conversion is essential for the long-term performance of the AD measurement card. Therefore comprehensive tests with the prototype boards have been performed and are still ongoing. We have observed rather rapid changes of ADC characteristic during the first 100 operating hours, after that, the errors became quite stable. Therefore, the cards must be operated for approximately one week prior to calibration (burn-in).

There are further tests ongoing, which shall answer the questions regarding long-term drift behaviour (1 year) and/or necessary recalibration intervals. So far, the results are in accordance with the theory, but final results are not yet available.

As the reproducibility is a crucial requisite for any high-precision measurement, we have also performed detailed tests on that issue. The same ADC card was analysed 40 times using the method mentioned above, the results are presented in fig. 5. The top and middle graphs show the computed offset and gain error respectively. The offset varies by 40µV (2ppm) and the gain error by 5ppm. The third graph in fig. 5 shows the 40 INL/DNL correction functions (gain error removed in advance) over the entire ADC range. The curves are reproducible within 0.5 LSB (2ppm). Different cards show different correction functions, so each individual card has its own fingerprint.

CONCLUSIONS

The presented ADC card - together with the analyzing and calibration method - offers excellent precision as well as stability and reproducibility characteristics, which are in the same order of magnitude as those of commercially available high-precision current transducers. The error functions are highly reproducible, stable and hence corrigible. Together with the controller card, a very powerful control platform for the next generation of power electronic devices for accelerator applications will be available.

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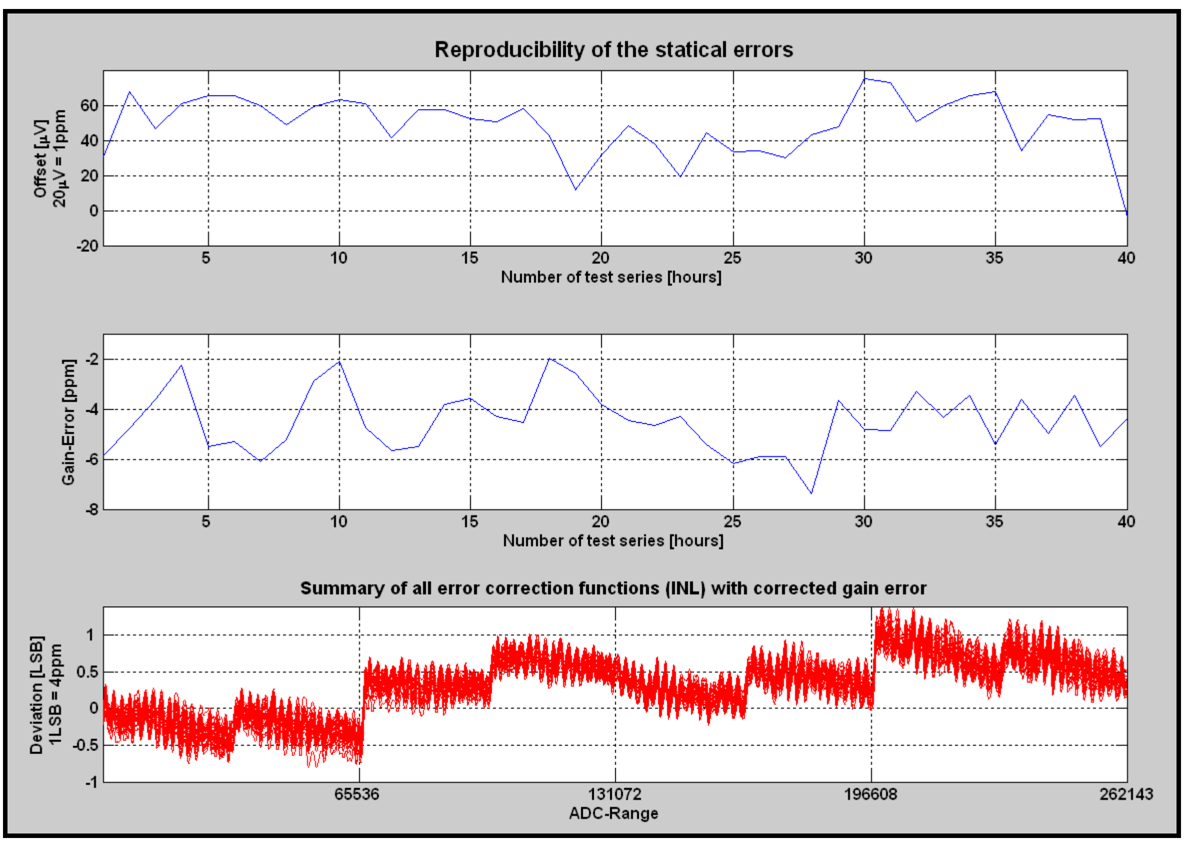

Figure 5: Reproducibility of the errors of the ADC-card.