BUNCH BY BUNCH FEEDBACK BY RF DIRECT SAMPLING

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Abstract

The direct sampling of RF signal from a beam position monitor is performed by the bunch-by-bunch feedback. With this scheme, the baseband conversion stage is eliminated, which leads to the simplicity and the low cost of the system, and the easiness of the setup and tuning.

INTRODUCTION

Recently, direct sampling of RF signal by ADC is widely used for detection of amplitude and or phase of the signal to detect the beam position [1] or for low-level RF control [2]. In SPring-8, we apply the RF direct sampling method to bunch-by-bunch feedback system to sample the peak of wideband bipolar signal from a beam position monitor electrodes to eliminate the down conversion stage.

RF DIRECT SAMPLING FOR BUNCH-BY-BUNCH FEEDBACK

The scheme of the RF direct sampling in comparison with the down conversion scheme is shown in Fig. 1. The bipolar RF signals from electrodes of a beam position monitor (BPM) are sent to an 180deg. hybrid to produce the difference signal (Δ). In conventional systems, this signal Δ is down-converted by a mixer with a harmonics of RF acceleration frequency f_{RF} to the baseband signal from kHz to a half of f_{RF}. Then the baseband signal is sampled by ADCs in a digital bunch-by-bunch feedback processor.

If the analog bandwidth of ADCs is wide enough to cover (1-1/2) f_{RF} to (1+1/2) f_{RF}, ADC can sample the peak voltage of the bipolar signal from the BPM and we can eliminate the down conversion stage. The RF acceleration frequency of the SPring-8 storage ring is 508.58MHz and the required frequency band is 254MHz ~ 762MHz for the RF direct sampling of the BPM signal.

For the ADC of the SPring-8 digital feedback processor [3], we chose Analog Devices AD9433 of which analog bandwidth is 750MHz full power. We use four ADCs to achieve the sampling rate 508.58MS/s though the maximum sampling rate of the ADC is 125MS/s, and the ADCs operate slightly higher sampling rate than the specification.

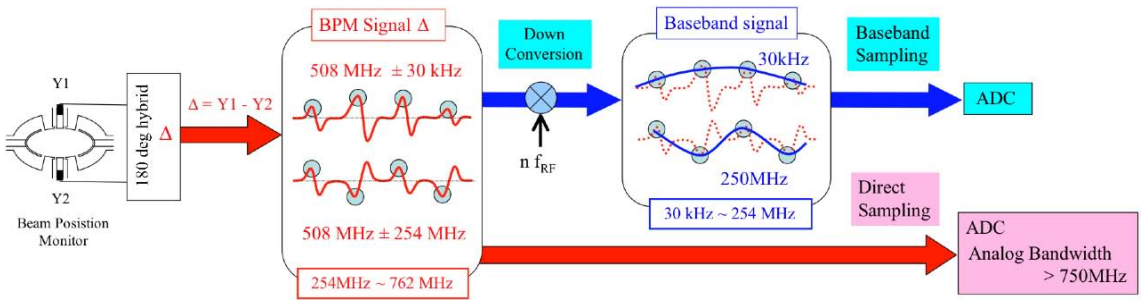


Figure 1: RF direct sampling scheme and down conversion scheme.

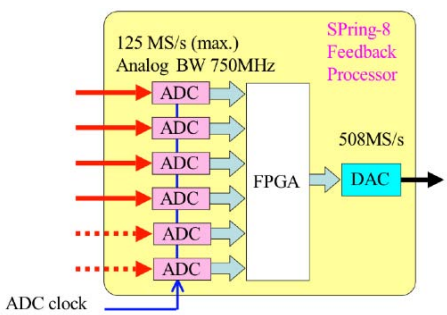


Figure 2: Architecture of the SPring-8 bunch-by-bunch feedback processor. The effective sampling rate of ~ 500MS/s required for the bunch-by-bunch feedback of the SPring-8 storage ring is performed by four or six ADCs of which maximum sampling rate is 125MS/s.

TIME DOMAIN TEST

The bench measurement of the time domain response of the ADC of the feedback processor was performed with a test signal which simulates the bipolar signal from a BPM. The setup is shown in Fig. 3. The clock pulse/generator produces rectangular pulses of 300 ps wide. This signal is send to a T-type connector one of which port is shorted to reflect back the signal with inverted polarity. The signal of the output port is the sum of the two signals: the signal come directly from the input port and the inverted signal from shorted port with time delay of ~100ps, and is the bipolar signal similar to the signal from a BPM. The bipolar signal is sent to one of the ADCs of the feedback processor. We measured the DAC output voltage changing the delay of this input signal to the ADC. A low pass filter (LPF) of Mini-circuits VLFX-780 is used to limit the bandwidth of the signal to fit to the analog bandwidth of the ADC. The results are shown in Fig. 4

and 5. Because the frequency band of the pulse/clock generator is up to 3.4 GHz, the 933 MHz low pass filter, Pico Second Pulse Lab. PSPL-5195, is attached to the output of the pulse/clock generator to reduce the frequency band to avoid the saturation of the amplifier. This filter, PSPL-5195, can be used to simulate the cable loss as shown in Fig. 6.

In Fig. 5, if the sampling timing is adjusted to the positive peak, then at the sampling timing for the next bunch after 2ns, the signal voltage is not zero but 8% of peak value. This is the same as the 2-tap FIR filter:(a_{-1} = 0.08, a_0 = 1) and the reduction of the gain at 250MHz is 16 %. The variation of the phase shift is small and less than 5 degree. If the sampling timing is shifted to 200ps earlier, the signal voltage at the timing 2ns after the sampling is zero and the gain reduction at high frequency is negligible.

Also the frequency response of the ADC with the input of sinusoidal waves was measured and the result is shown in Fig. 7. This result shows the raise of the gain above 800 MHz which is beyond the frequency of the analog band width of the ADC. The LPF (VLFX-780) reduces the signal level in this region as shown in the frequency spectrum of the test signal shown in Fig. 8.

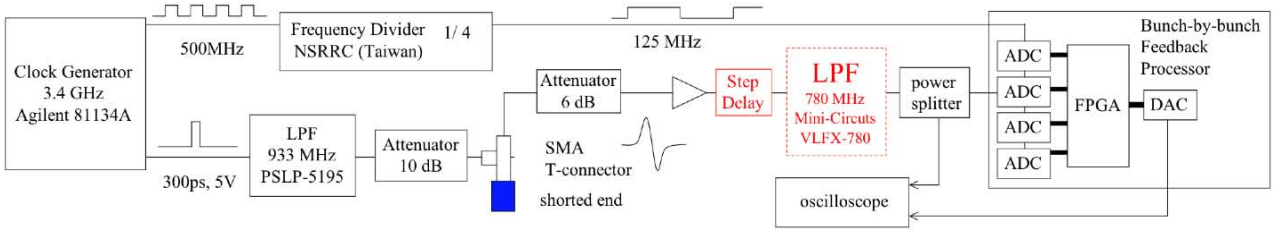


Figure 3: The setup for time domain response measurement of ADC of the feedback processor. The input to the ADC and the clock for ADC is synchronized. The delay of the sampling timing is changed by the step delay and the measurement is performed with LPF (VLFX-780) and without LPF.

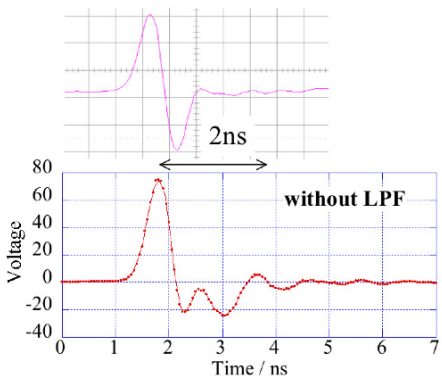


Figure 4: The test signal without LPF for the input to ADC (top) and corresponding DAC output voltage (bottom). The horizontal scale is converted from delay value to show the time dependence.

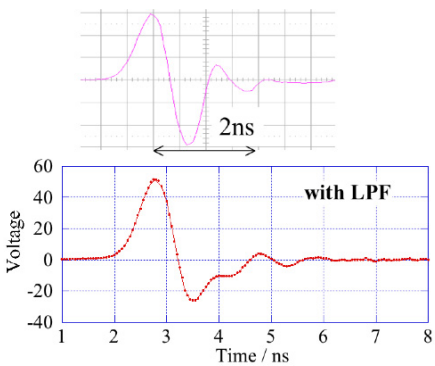


Figure 5: The test signal with LPF for the input to ADC (top) and corresponding DAC output voltage (bottom). The horizontal scale is converted from delay value to the time dependence.

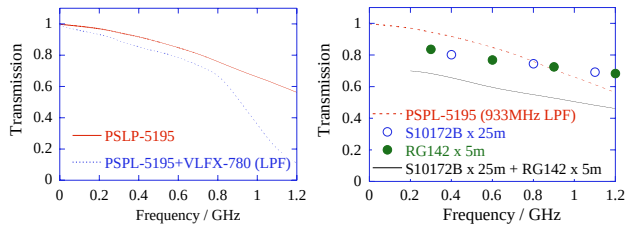


Figure 6: (left) Frequency response of the LPF (VLFX-780) and the low pass filter PSPL-5195 attached to the output of the pulse/clock generator. (right) Frequency response of the filter, PSPL-5195, and the cables, S10172B x 25m and RG142 x 5m. Those two cables are used in series from the BPM to the feedback system in SPring-8.

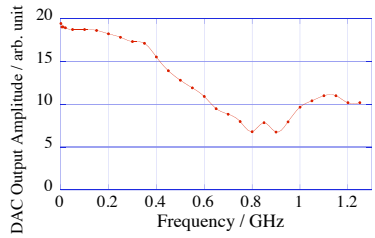


Figure 7: Frequency response measured by sinusoidal input signal to ADC. The raise of the gain above 800 MHz can be seen.

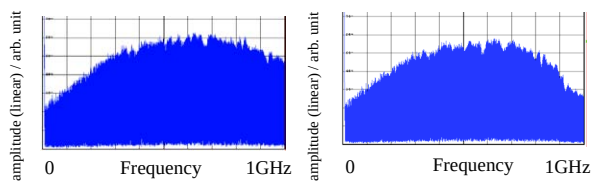


Figure 8: Frequency spectrum of a test signal without LPF (left) and with LPF (right). Vertical scale is linear. The spectrum is the spikes of harmonics of repetition frequency of the test pulse.

EFFECT OF JITTER

In RF direct sampling, the ADCs sample high frequency analog signal and the effect of the jitter of the sampling timing of the ADC is larger than the baseband sampling. In an ideal system, if the feedback is turned on, the beam is stable and no signal is coming from a BPM to a feedback. However, in actual, even the beam is stable, we can observe the residual signal from the BPM as shown in Fig. 9 and this signal height is corresponding to 100μm in SPring-8 and the jitter produces the noise from this signal as shown in Fig. 10. The jitter is observed at the measurement of Fig. 4 and Fig 5 as a noise voltage at zero crossing timing and is 12 ps (peak to peak). Then, the rms value of the jitter should be less than 6ps. This value is consistent with the estimated jitter of the frequency divider [4] offered by NSRRC, Taiwan. In SPring-8 case [5], this jitter produces the noise corresponding to 3μm and the resultant beam motion excited by the noise is 0.3μm, which is quit small compared with the vertical beam size, 5μm.

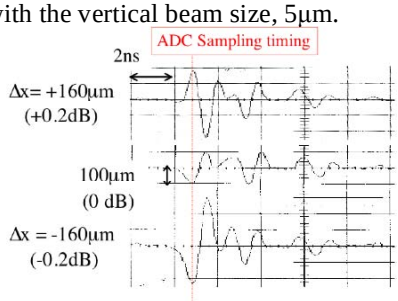
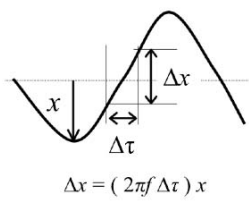


Figure 9: The trace in the center is the residual signal of the difference signal (Δ in Fig. 1) after the adjustment of variable delays and attenuators in SPring-8. The top and bottom traces are the signals produced by the change of the variable attenuator by 0.2dB, which corresponds to the beam position shift of 160μm. The peak height of the residual signal is corresponding to the beam position shift of 100 μm



Resolution of BPM
Frequency f = 1 GHz
Jitter σ_τ = 5 ps
residual signal x = 100 μm
σ_x = (0.03)× 100 μm = 3 μm
⇒ beam motion 0.3 μm
(SPring-8 case)

Figure 10: Noise produced by residual signal and jitter.

APPLICATION TO SPRING-8

We applied the RF direct sampling scheme to the SPring-8 feedback system and the system is in operation from the beginning of 2007. We obtained the damping time 0.2ms in low frequency and 1.5ms in ~250MHz [6]. The setup of the RF direct sampling is shown in Fig. 11 and the square wave mixing scheme [7] for the down conversion used until the replacement to the RF direct sampling is shown in Fig. 12. A possible down-conversion scheme is also shown in Fig. 13. With RF direct sampling scheme, we eliminated the down-conversion stage which is composed of mixers, an amplifier and components for LO signal conditioning for mixing, and baseband amplifiers. Then the reduction of the tuning points, the number of components and the cost are accomplished and we obtain the easiness of the tuning.

The RF direct sampling scheme will be applied to Hefei Light Source.

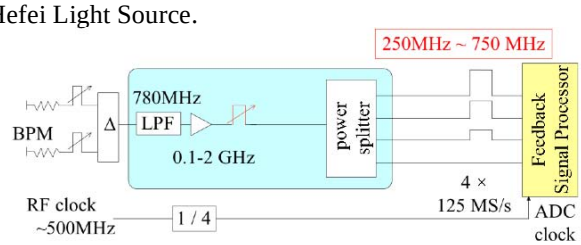


Figure 11: RF direct sampling

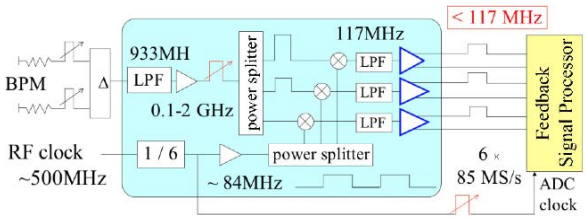


Figure 12: Square mixing scheme used before in SPring-8

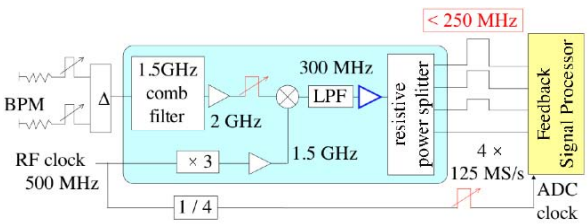


Figure 13: Possible down conversion scheme for SPring-8

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[4] Courtesy of K.T.Hsu and D. Lee, NSRRC, Taiwan.

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