Digital Low Level RF

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Outline

1. Introduction
2. State-of-the-art: system design
3. State-of-the-art: algorithms
4. Different designs overview
5. Summary

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1. **Introduction**
   - Basics
   - From analogue to digital
   - Digital vs. analogue
2. State-of-the-art: system design
3. State-of-the-art: algorithms
4. Different designs overview
5. Summary

Intro: basics

DLLRF = any system with important digital features

- Preferred choice for (complex) new developments.
- Prompted by accelerator requirements: performance/reliability, diagnostics, remote control, multi-user operation…
- Enabled by digital/telecoms progress:
  - high-speed processing
  - fast conversion
  - highly linear chips…
- Analogue (low-latency) & digital loops in parallel (e.g. LHC)

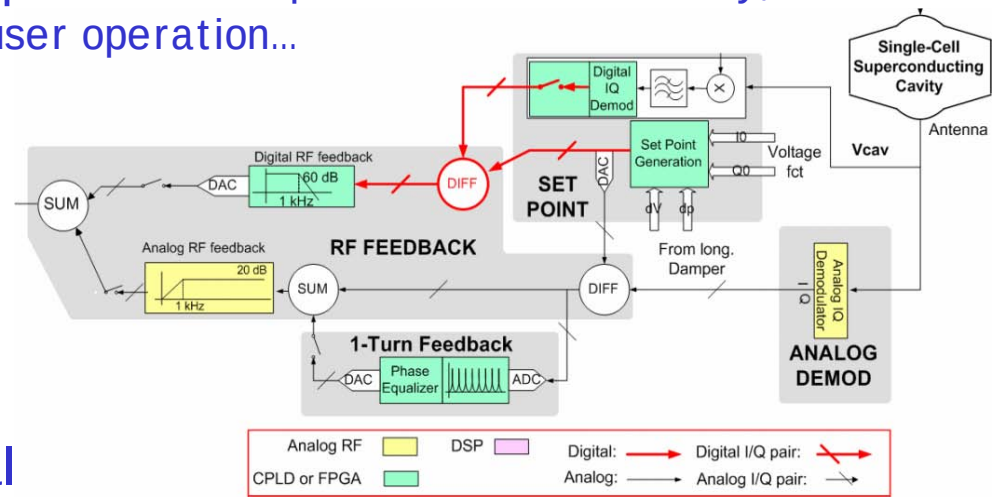


Figure 1: LHC RF Feedback loop [TUPCH195, P. Baudrenghien]

- New machines with analogue LLRF:
  - Daresbury ERLP: soon to test DLLRF [TUPCH151, A. Moss et al.]
  - Diamond Storage Ring [TUPCH192, A. V. Watkins et al.]
  - SOLEIL: soon to become DLLRF [TUPCH186, P. Marchand et al.]

Intro: analogue → digital

'70s: µ-processor control

'80s: NCO replaces VCOs

- High stability/resolution …
- Master/slave schemes.

Digital filters (ex: combs)

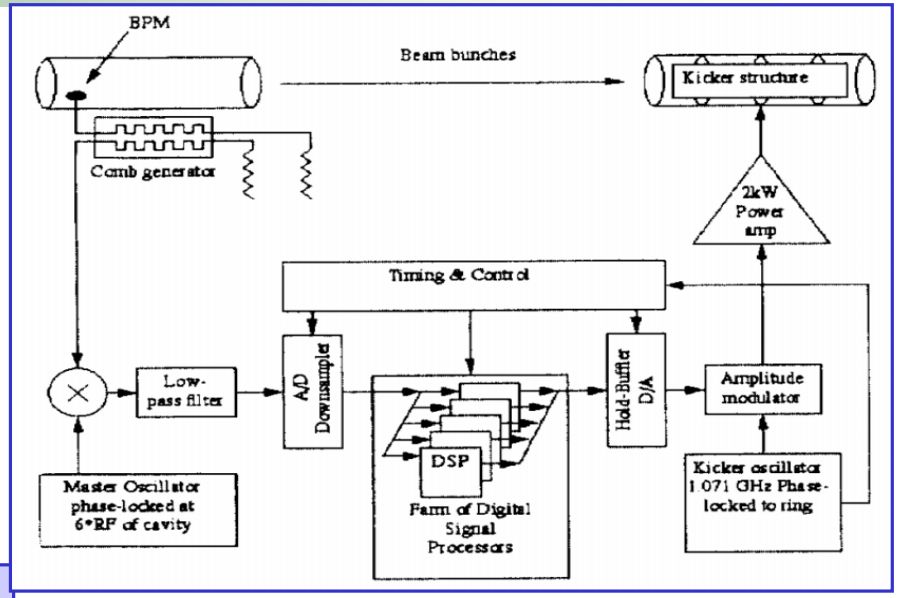
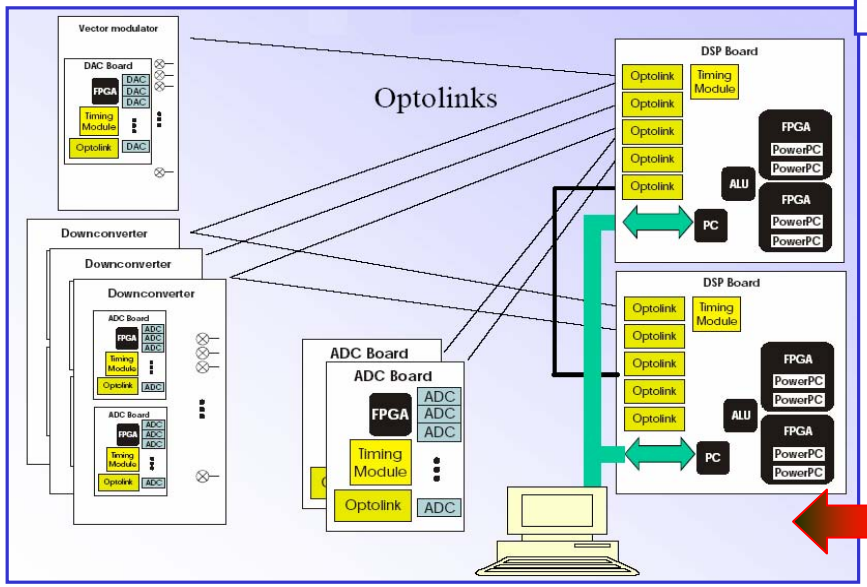


Figure 2: Bunch-by-bunch longitudinal feedback system for PEP-II.

'90s: DSPs + complex algorithms



Now: DSPs/FPGAs/optolinks …

Figure 3: Third generation hardware for TTF-UVFEL.

Intro: digital vs. analogue

	Digital	Analogue
Implementation	Learning curve + s/w effort	Easier/known
Latency	Longer	Short
DAQ/control	I/Q sampling (also direct) or DDC	Ampli/phase , IF downconversion
Algorithms	Sophisticated. State machines, exception handling…	Simple. Linear, time-invariant (ex: PID)
Multi-user	Full	Limited
Remote control & diagnostics	Easy, often no additional h/w	Difficult, extra h/w
Flexibility / reconfigurability	High (easier upgrades) [TUPCH190, S. Simrock et al.]	Limited
Drift/tolerance	No drifts, repeatability	Drift (temperature..), components tolerance
Transport distance without distortion	Longer	Short
Radiation sensitivity	High	Small

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2. State-of-the-art: system design

- Custom vs. COTS
- DSP & FPGA
- I/Q detection

3. State-of-the-art: algorithms

4. Different designs overview

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SoA design: custom vs. COTS

	Custom	COTS
Development time	Longer: learning curve + high-speed digital design + s/w efforts	Shorter / easier planning
Flexibility	Can target several accelerators	Little (daughtercards help)
Obsolescence	In-house knowledge: possible design upgrade with minimal changes	Manufacturer dependence

- Most systems include custom boards.
- Inter-labs collaboration helps custom design:
  - SLAC/LBNL/INFN-Frascati: longitudinal digital feedback.
  - ORNL/LANL/LBNL: SNS linac DLLRF.

Examples: **COTS**: J-PARC Linac

Custom: LHC (> 300 modules, 23 types).

SoA design: DSP & FPGA

DSP

- Fast & complex processing
- Sequential/parallel (e.g. SIMD)
- Interrupt-driven (no RTOS), assembly/C/C++/high level

FPGA

- Faster processing + general logic
- Parallel
- Proprietary/VHDL-Verilog/high level [TUPCH196, J. Molendijk et al.]

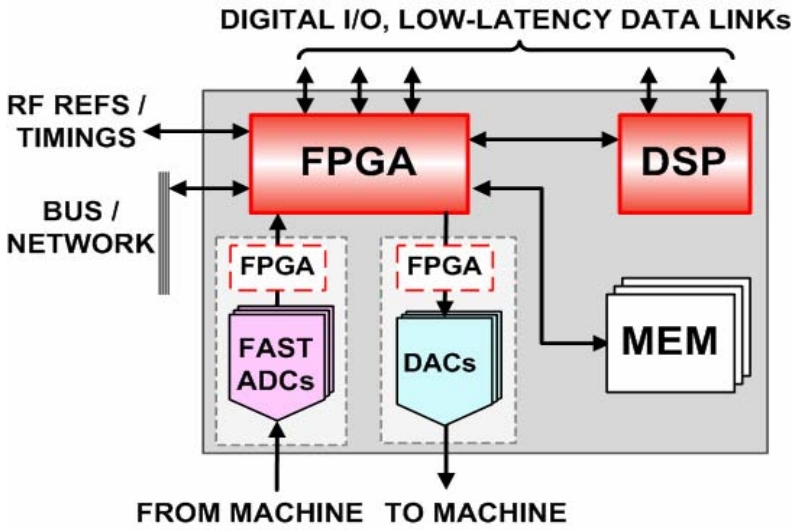

Figure 4: General DLLRF board.

- Daughtercards → modularity
- Memory: SRAM + DRAM
- Platform: crate vs. Network Attached Devices (NAD)
- Many low-latency links (Infiniband, RapidIO, Aurora, linkports …)

Examples: BNL, CERN.

SoA design: I/Q detection

I/Q detection, processing & control suited to DLLRF.

Digital Down Converter (DDC)

- FPGA-implemented (COTS: long group delay).
- Improves SNR & provides data reduction.
- Flexible & suited for high f_{REV} swings.
- Used by: CERN LEIR, SNS ring, Fermilab's Main Injector …

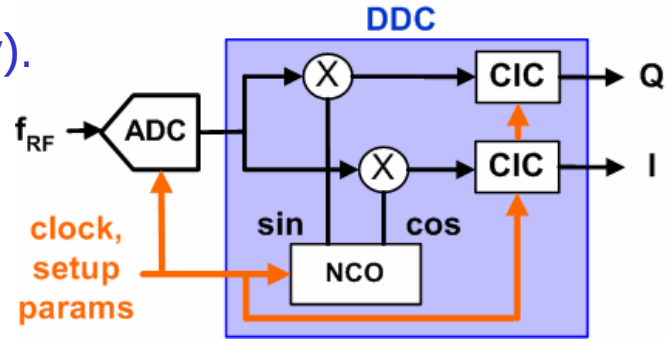

Figure 5: DDC scheme.

I/Q sampling

- Simple/low latency scheme (special DDC case).
- Sensitive to ADC noise -> increase sample nb /synchronous period
- Used by: CERN Linac3, CESR, LHC...

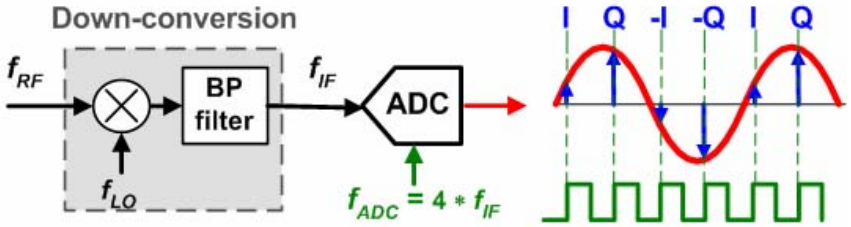

Figure 6: I/Q sampling scheme.

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2. State-of-the-art: system design

3. **State-of-the-art: algorithms**
   - Implementation
   - Modern control

4. Different designs overview

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SoA algorithms: implementation

❖ **Biquad**: PID + IIR + building block for high-order filters.

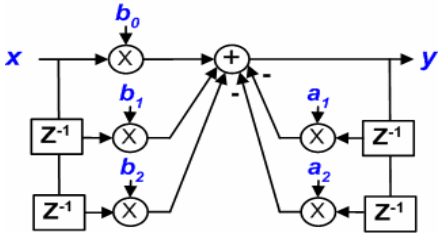

Figure 7: Direct Form I

Fixed-point DSP

FPGA /Floating-point DSP

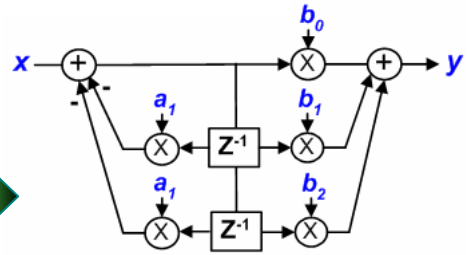

Figure 8: Direct Form II

❖ **Trigonometric functions**: loops + DDCs.

FPGAs: CORDIC. **DSPs**: polynomial interpolation (high-resolution).

❖ **Cascaded Integrator-Comb (CIC)**: DDCs

- low-pass, multirate filter
- 3 control params: ***M***, ***N***, ***R***
- FPGA-implemented (few resources needed!)

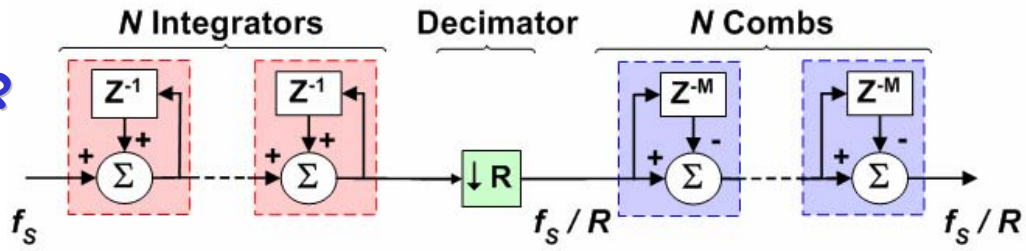

Figure 9: Decimating CIC structure.

SoA algorithms: modern control

MIMO/time-varying/non linear system → modern control techniques.

- SLC: pioneer for modern control in feedback systems (ex: adaptive cascaded feedbacks).
- State-space formalism: feedback design from system internal state.

  Ex: BNL's RHIC/AGS, LHC.

- Adaptive feedforward (AFF): controller modified thru' history data .

  Ex: SNS linac beam loading compensation.

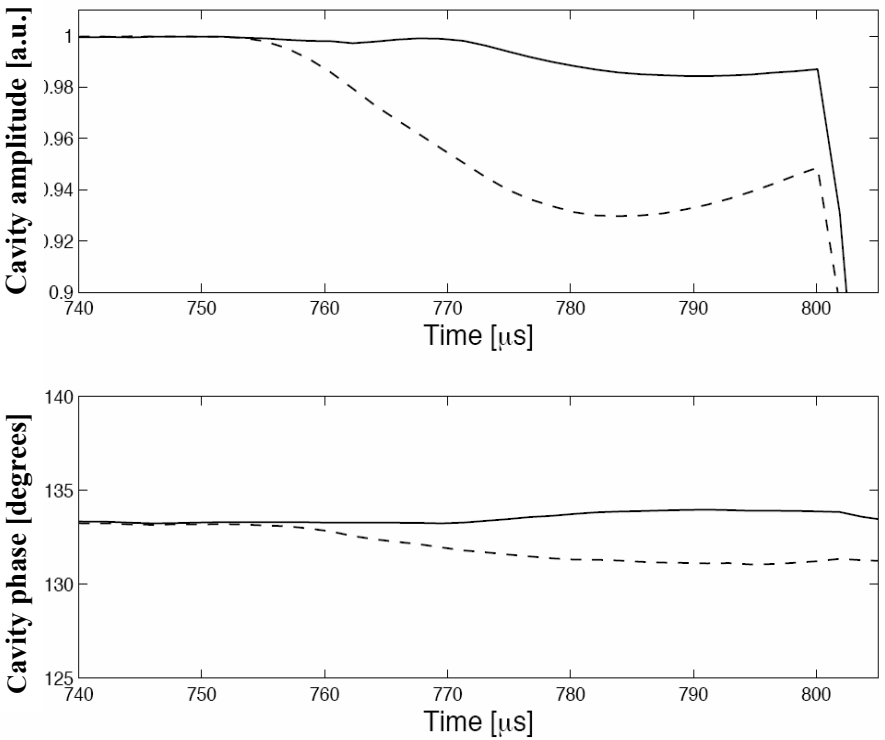

Figure 10: Cavity amplitude/phase under beam loading with (solid line) & without (dashed) AFF. (K. Kasemir et al, PAC'05.)

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4. **Different designs overview**
   - Cyclotrons, synchrotrons & hadron colliders
   - Linacs, FEL & linear colliders
   - Light sources & lepton colliders
5. Summary

APOLOGIES FOR DESIGNS NOT MENTIONED HERE!

Cyclotrons, synchrotrons & hadron colliders

	Type	What	How
TRIUMF	*Cyclotr.*	Cavity amplitude loop	Motorola DSP
CERN LEIR	*Synchr.*	Phase/radial/synchro loops. Cavity amplitude/phase loops (2 harmonics), to be finalised	VME64x boards/daughter cards. SHARC DSPs/Stratix. Digital I/Q (CIC) + tagged clock.
FNAL Main Ring	*Synchr*	Phase/radial loops. Digital long./transv. bunch-by-bunch feedback.	VXI crates + SHARC DSPs; FPGAs for long/transv, feedback.
SNS Ring	*Storage ring*	1 ms accumulation period. Cavity controller amplitude/phase (PI). Slow cycle-to-cycle beam feedback (FEC).	EPICS + COTS PMC daughtercards (Quad SHARC DSPs).
J-PARC RCS + MR	*Synchr.*	High intensity beam, MA cavities & vector sum. Multi-harmonic RF generation for acceler. & shaping. Phase/radial/AVC loops. Feedforward (beam loading). [TUPCH193, A. Schnase et al. TUPCH130, F. Tamura et al.]	EPICS, FPGAs. Reflective memory. Cascaded CIC with smoothly changing coeffs.
FNAL Tevatron	*Hadron collider*	Phase/radial/collision point by feedforward.	VXI+SHARC DSP
RHIC	*Hadron collider*	Phase/radial/synchro loops with state-variable formalism.	Custom/COTS boards (SHARC DSPs).
LHC	*Hadron collider*	Cavity tuning + power & beam control, RF synchro & long. damping. [TUPCH195, P. Baudrenghien]	VME + TigerSHARC + FPGA. >300 modules of 23 types.

Linacs, FEL & linear colliders

	Type	What	How
SNS	*pulsed*	GDR, NC + SC cavities. Fast feedback (PI) + adaptive feedforward. [TUPCH198, L. Doolittle et al.]	EPICS, Xilinx FPGA
VUV-FEL	*pulsed*	GDR + vector sum. Feedback/feedforward. [TUPCH189, W. Koprek et al.]	DSPs + gigalink channels. (SimCon3.x boards)
J-PARC	*pulsed*	GDR, fast feedback + resonance cavity control. Under commissioning.	EPICS, COTS cPCI; DSP + FPGA.
CERN Linac3	*pulsed*	PI controller.	VME + FPGA
PEFP	*pulsed*	Cavity field fast feedback.	EPICS + ADI Blackfin + Xilinx FPGA.
CEBAF	*CW*	GDR, single-cavity control.	VXI + Stratix FPGA.
Cornell ERL	*CW*	Under way (tested @JLAB ERL). GDR, extremely high Q_L (10^7-10^8) → small cavity BW (few Hz).	I/Q sampling. FPGAs + SHARC DSPs (as for CESR)
ISAC II	*CW*	SEL controller, SC cavities. Amplitude/phase detection, I/Q control. [THPCH106, M. Laverty et al.]	Mixed analogue/digital with Motorola DSP.
ILC	*Linear coll.*	Implementation(s) under discussion. Field stability requirements: 0.1% amplitude, 0.1 deg phase.	Different DLLRF system being proposed.
CLIC	*Linear coll.*	Feasibility study. Precise phase driving field stability needed (phase). [TUPCH086, J. Sladen at al.]	DLLRF with FPGAs with fast feedforward to be used.

Light sources & lepton colliders

	Type	What	How
ELETTRA + SLS	*Light source*	Transverse/Longitudinal bunch-by-bunch feedback.	COTS board + TI DSPs.
PEP-II	*Lepton collider*	NC cavities. Active cavity impedance reduction by analogue direct RF feedback + digital comb filters + digital gap feedback. Digital long. + transv. feedbacks.	EPICS, VXI, baseband processing.
KEKB	*Lepton collider*	SC + NC (ARES) cavities. Passive cavity impedance reduction. Digital bunch-by-bunch feedback.	COTS board + TI DSPs.
Cornell's ESR	*Lepton collider*	Field control system; high beam loading, feedback & feedforward.	I/Q sampling. FPGAs + SHARC DSPs.
DAFNE	*Lepton collider*	Digital transverse/longitudinal bunch-by-bunch feedback	AT&T DSP1610 DSP + dual-port RAM.

Summary

- DLLRF has many appealing factors: diagnostics, remote-control, multi-user, complex algorithms … difficult with analogue LLRF.
- Widespread use & preferred choice for new developments.
- Analogue LLRF used for fast loops. Technology progress will close gap soon(ish).
- Many trends h/w + s/w (standardisation?).
- Good possibilities for inter-labs collaboration.

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