THE STARBURST, A J-11 BASED FRONT-END PROCESSOR SYSTEM

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Abstract

This paper will describe a coherent solution to the demand for ever-increasing performance in CAMAC-based data acquisition and pre-processing systems. It will outline the development of this modular high density system, covering the design decision and trade-offs from the hardware and software standpoints. Current applications will be briefly described and the direction of future developments will be indicated. The keystone of the system is a single-width module based on a DEC J-11 processor. It offers all the functions of an Auxiliary Crate Controller with programmable LAM-grader; at the same time functioning as an autonomous computer with a high-speed 64K word dual-port memory, console and Q22-bus peripheral interface. This structure supports extension on both, the CAMAC side and the Q-bus side; and the hardware design choices have been made with a view to allowing use of a large range of popular software. The principal module is supported on the CAMAC side by dedicated semi-autonomous memories, and on the computer side by portable winchester and floppy disk storage subsystems, while offering expansion capabilities through the Q22-bus port. Current applications in the fields of host-computer front-ends, stand-alone test systems, portable workstations and embarked data-loggers will be described.

Introduction

The complexity of high and low energy physics experiments has increased significantly over the past years to bring about the need for sophisticated on-line decision making hard- and software, exhibiting very high process power capabilities.

The "Starburst" has been designed to fulfill this criterium, while maintaining stability of both hard- and software costs.

These design targets have been achieved:
- speed
- ease of operation
- use of well proven software.

Speed target

Until recently data acquisition and reduction rates of 1 MIPS and greater were only possible employing two known techniques:

- DMA transfers via connections to large host computers
- or through special hardwired or bit slice dedicated processor connections.

The former solution suffered from being very expensive while the latter solution based on the reduction of data locally (which was correct in theory) proved to be difficult and costly to maintain, since it required highly skilled hard- and software support staff.
The "Starburst" system design concept had to meet a well balanced speed versus cost compromise.

Ease of operation goal

The processor had to be user friendly for engineers and physicists alike allowing for easy operation without the special knowledge of complex programming techniques.

The CAMAC side of the interface had to be very simple from a hard- and software operational point of view: i.e. the loading of application programmes, acquisition and reduction of data and the in-out transfer to the host machine. Unrestricted access to the total memory recourses had to be provided as well. Changes to and expansion of application programmes had to be kept simple. Synchronisation between different processors had to be achieved with ease.

Software target

Although it was essential to optain maximum processing speed with this new CPU, it was nevertheless a must to enable use of all prewritten and off the shelf software. It was our goal to allow software written and generated on large host machines to be employed with ease on the "Starburst".

In summary: The "Starburst" meets all the aforementioned prerequisites. While offering this high performance to a modest entry level person (through its ease of operation and implementation), the expert user will find almost limitless features ready to be explored within "Starburst".

The Starburst Structure

The Starburst module main features are:

- DEC J-11 16/32 bit 200ns-cycle processor with PDP 11/70 performance
- on-chip memory management to address up to 4 Mbytes of memory
- floating point instructions in single and double precision
- Auxiliary Crate Controller logic
- 64K word 16 bit dual-port memory
- high-speed static RAM (100ns) or EPROM mixed configurations

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- DEC compatible console interface
- Q-bus output in Q22 format.

Great attention has been given to the flexibility in the design:
The memory, CAMAC, peripherals, Q-bus and other dynamic parts of the board are controlled by PALs (Programmable Array Logic) to ensure fastest response times and easy system tuning.

The most important feature is its DEC software compatibility. Programmes written for PDP 11 or LSI 11 hardware can be executed on the Starburst. (The on board 64K word memory can be supplemented with additional memory via Camac or Q-bus if necessary.)

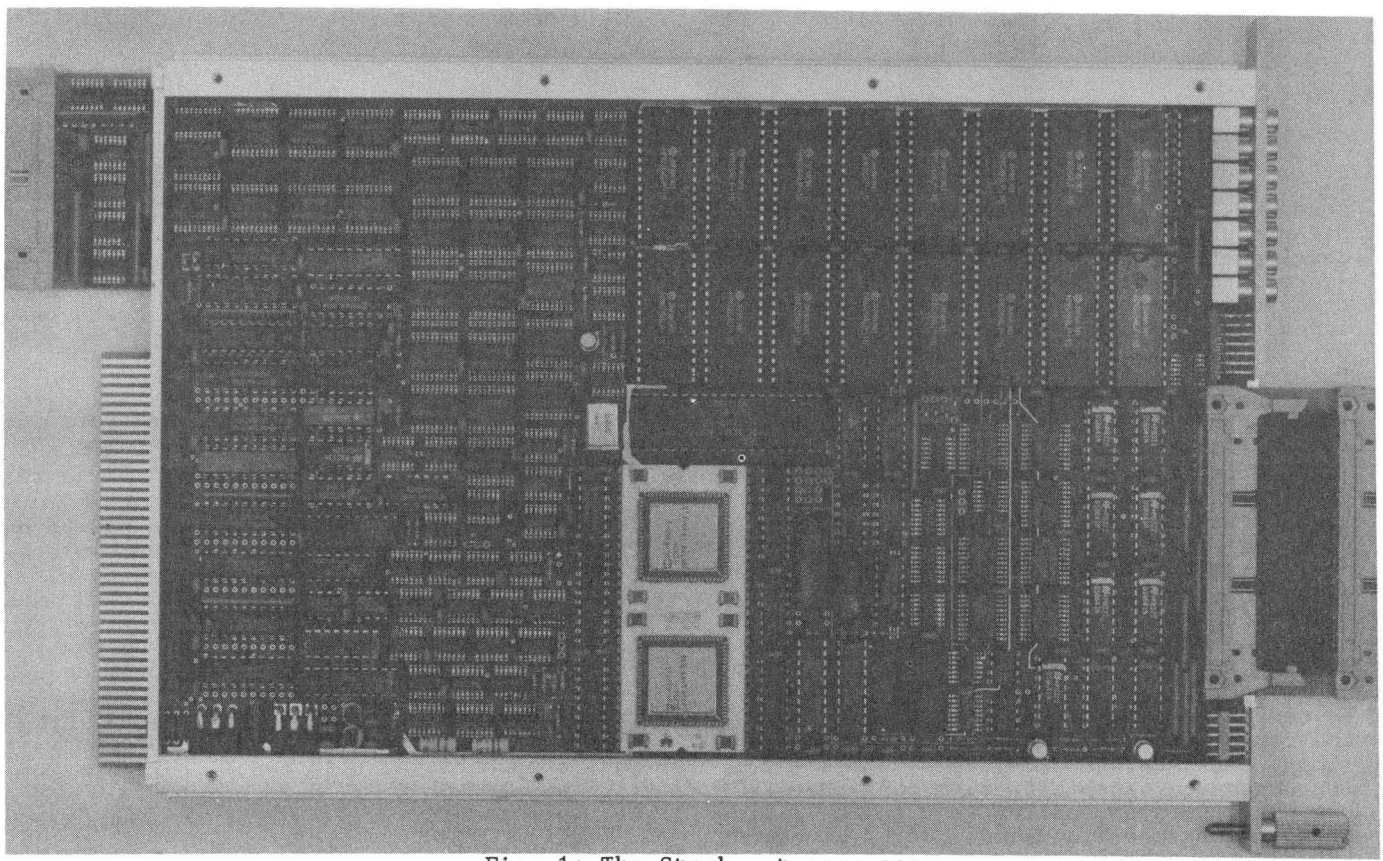

Fig. 1: The Starburst processor

The CPU

The J11 is the first high-speed processor of its kind to be released by DEC using single package VLSI technology.

Although this CPU emulates the PDP11/70, it is significantly better for contest switching uses than its mainframe counterpart. Running this unit at the 20 MHZ clock rate, performance levels of 200ns for read and 400ns for write operations are achieved.

Timing for some standard instructions are as follows:

Integer performance	Time	Floating point perf.	Time
ADD RØ, R1	200ns	ADD ACØ,AC1	6.8us
ADD #n, RØ	400ns	MUL ACØ,AC1	11.6us
MOV @RØ,@R1	1000ns		

Due to the pipelined structure of the memory management system built into the chip, the above figures apply throughout the total memory range (4MB) provided fast memories are employed.

A further enhancement to overall speed is through the use of a high-speed floating point booster, connected to the co-processor bus of the J11.
Speeds of 1 to 4 us for floating point operations should be possible.

The Memory System

The on-board memory bank features a 128Kbyte dual-port memory.

Memory organisation. The memory is organized in 64Kwords. It is laid out in blocks of 8Kbytes with two blocks forming an 8K 16bit memory bank. Blocks can be assigned either to RAM chips or EPROM chips. The RAM chips are fast static RAMs which provide the highest possible access speed (100ns available to date). The EPROM chips are 8Kbyte chips of the 2764 type. Since the EPROM and RAM chips are pin compatible, the memory organisation is very flexible.

Dual porting. The total 128Kbyte memory locations are fully accessable through two independent ports with one dedicated to CAMAC and the other to CPU operations.

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Both have their own private read/write pointers.
The CPU is unaware of this dual port architecture, thus to the program the memory looks like a normal memory bank.

CAMAC port. The CAMAC port has two access commands available:

- memory read/write commands with automatic memory address incrementation (for program loading and data retrieving)
- memory read/write commands without memory address incrementation (for mailboxes and multiprocessor applications).

Memory Expansion. Memory capacity can be expanded on the Q-bus and/or Camac side of the Starburst. Dedicated high-speed memories of the histogramming and list mode type can be connected to the Camac side, they appear to the Starburst as second memory banks. Due to the high speed and simple design (memory-mapped addresses) of the CAMAC access, operation is as fast as Q-bus attached memories. The Q-bus port will drive any memory that meets DEC Q22 specification. Since the Q-bus interface is driven by PALs, it too can be tuned as required. Q-bus memories can reside in a specially developed Camac housed mini back plane (see Fig.2).

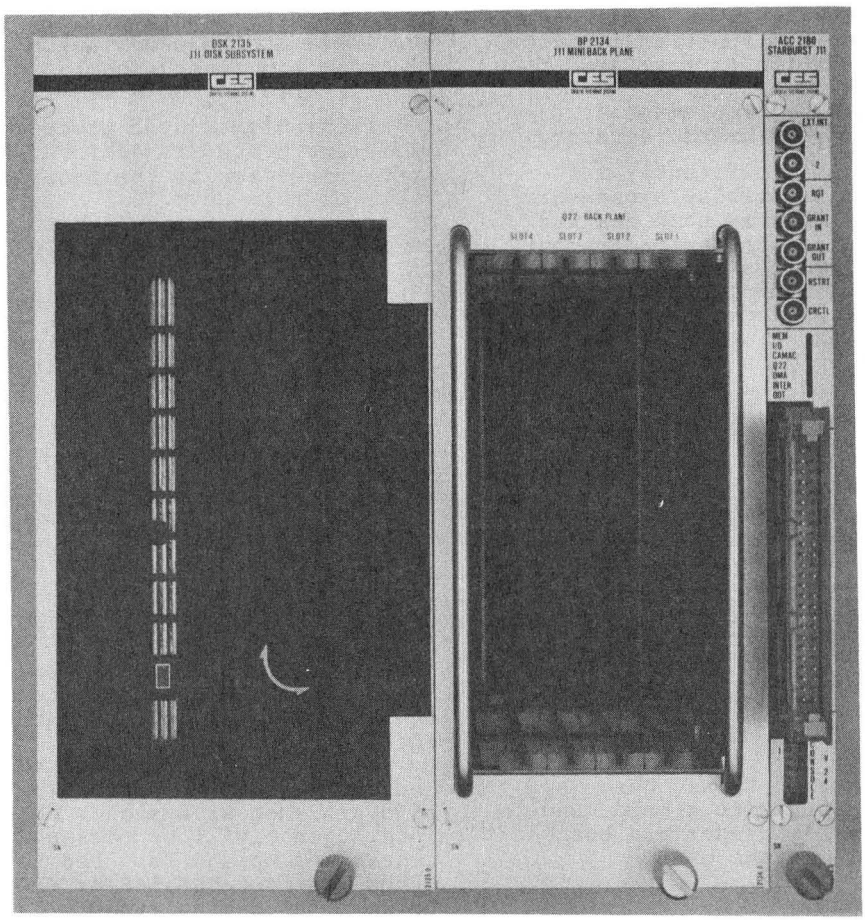

Fig. 2: A Stand-Alone configuration with mini back plane and disk subsystem.

The CAMAC Interface

All CAMAC addresses are memory mapped, this feature ensures maximum throughput. A CAMAC command can be executed using only one MOV instruction. Furthermore the Camac Interface incorporates an overlap processor which significantly enhances the overall performance of the Starburst.
The Camac Interface is used in three modes of operation:

1 - loading the program from the host via the Camac branch into the Starburst memory (front-end processing application only)
2 - running of the local data acquisition and reduction program
3 - sending the data via the branch to the host

Modes 1 and 3 involve Camac access from the host computer to the Starburst, while mode 2 involves Camac access from the Starburst to other crate stations.

Mode 1: Since Starburst is looked at by the host as just another passive Camac unit, Camac access to the processor is extremely easy. The program is loaded into

the memory as a binary file via the branch and the CPU is activated. No Q answer testing is required since the memory of Starburst is always faster than Camac.

Mode 2. Starburst can access any CAMAC station housed within the crate if connected to the following crate controllers:
- CCA2, SCCL2, DEC dedicated Crate Controller with ACB interface, System Crate Controllers and Dummy Crate Controllers (for Stand-Alone operation).

Camac stations in other crates can be accessed as well, provided a Camac branch driver is located within the Starburst crate.

The N and A parameters of the CAMAC command are I/O page addresses. The F parameter is sent to a memory mapped function register. Q,X and control information is retrieved from a memory mapped status register.
24 bit CAMAC transfers are implemented through an additional read/write register.

Since the J11 CPU runs significantly faster than the CAMAC cycle, an overlap processor has been implemented. However this feature is completely transparent to the programmer. The overlap CPU will process in parallel the CAMAC accesses and the program execution. This feature will release the CAMAC after S1 in worst case, thus making available at least 600ns to the CPU allowing it to proceed with program execution before the end of the CAMAC cycle. An overrun logic is implemented.

Mode 3. When all the data acquisition, reduction and formatting is finished, the Starburst signals to the host that the data is ready by raising its own LAM or writing a flag into a mailbox location.
The host computer then accesses the dual port memory from the CAMAC side by setting the read address pointer and sending the required number of read commands. The word count of the data block can also be used as an argument in a mailbox.

Interrupts and LAMs

The complete PDP set of traps, hard- and software interrupts along with a hard- and software programmable LAM grader are board resident and available to the user.
Interrupt sources:
- sum of LAM interrupt
- real time front panel interrupt
- software interrupt (from host to Starburst)
- Q/X error interrupt
- overrun interrupt (from overlap processor)

Each source is accessible as a bit in a memory mapped register and can be individually masked by a mask register.
Real time interrupts are used to activate a program upon reception of a given trigger.
Software LAMs are used to signal to the host or to another processor that the data is available for transfer.
Software interrupts are used to activate special host or additional Auxiliary Crate Controller routines.
The LAM grader is interfaced through Camac to simplify operation in a multiprocessor environment. Each LAM can be read, masked and unmasked using Camac commands.

Multiprocessor Starburst System

Since the Starburst is functionally an Auxiliary Crate Controller, several units can be plugged into the same crate and operated in a multiprocessor environment. In this configuration the processors communicate and synchronize themselves by employing the following methods:
- through CAMAC using the "Mailbox" approach
- through CAMAC using the "Software LAM" feature
- via the front console real time interrupt jack.

Priority between processors is established using the daisy chain mechanism. Data contained in the memory of any processor is available to the other units as an extension of their own banks, thanks to the dual port architecture of these memories.

Synchronisation of processors residing in different crates is achieved by direct interconnection to the front panel interrupts of each unit.
At the present time all data transfers between processors residing in different crates as well as transfers to and from the host are routed through the Camac branch or via the Q-bus interface boards.
A multiprocessor system using the Q22 bus (in high speed) is currently being investigated.

Since the Starburst processor uses programmed I/O mode for data handling (which is already faster than the CAMAC branch driver operating in the fastest DMA mode), most of the data reduction should be done at the Starburst level to reduce the number of branch transfers required.

The "Starburst" as a Stand-Alone Computer

The Starburst can also be operated as a Stand-Alone Camac Computer, since it is equipped with an onboard Q-bus- and console interface.
By attaching a terminal to the Starburst console connector and running EPROM resident software such as Basic or Forth, sufficient intelligence will be present to look after system set-up and test bed routines.
EPROM resident RSX-11S or MRRT-11 can also be used supporting fixed or application software. More complex applications requiring the use of a disk based operating system such as RSX-11 are possible when connecting a disk subsystem. For this purpose a Camac housed mini back plane can be cabled to the Q-bus connector of the Starburst. Q22-bus interface and the portable disk subsystem can be attached to the mini back plane resident Q-bus controllers.
Although the disk subsystem can be physically mounted in the Camac crate, it can also be shelf or rack mounted, since it has its own live supports build in.
The addition of a DEC Q-bus ETHERNET interface card can transform the system into a network connected remote terminal.

Applications

The most efficient use for Starburst is high-speed front-end processing. Typical applications include On-Line Beam Profile Monitoring in Accelerator Ejection Halls, ADC read-out in High Energy Physics, On-Line Pulse Height Acquisition and Display Systems in Nuclear Physics, Data preparation for control room displays in Accelerator Control, Position and speed control of Radar Antennas.

The second category of application is High Performance Data Acquisition Systems. The Starburst design concept (speed, compactness, ruggedness, ease of use) provides the user with the very best performance/density package such as required in Airborne Measurement Systems, Portable Rugged Data Loggers and Fast Fourier Transform Systems.
A complete pulse height analysis system is being developed around the Starburst.

The third application field is Intelligent Remote Network controlled workstations.

Conclusion

The most significant progress which has been made with the introduction of the Starburst is that the CAMAC standard can be used at its speed limits without any special software efforts nor special knowledge of complex hardware.

All the Sparse Data Scan software along with the more comlex micro programmed branch driver control routines, can now be replaced by a simple straight forward Starburst resident software and a host resident read out programme, talking only to one station in each crate, activated by a LAM and uncorrelated to timing considerations.

The possibility to operate several Starburst processors in a crate offers a new degree of freedom in system design.

Since the introduction of these machines one thing has become evident:
In large systems the bottleneck now resides on the branch transfer side. Since the branch is much less active when employing the Starburst, the bottleneck effects are less noticeable, however a faster read out data transfer method between the ACC memory and host computer needs to be investigated.

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