NEW GENERAL PURPOSE INTERFACING MODULES FOR ACCELERATOR CONTROL SYSTEM

K. Shimizu, T. Wada, J. Fujita and I. Yokoyama

The Institute of Physical and Chemical Research (RIKEN) Wako shi, Saitama 351, Japan

Summary

Two types of intelligent interfacing modules for controlling many apparatus are designed. They can be used as an interfacing system which connects a CAMAC crate or a host computer with various controlled apparatus. They can also be utilized as an intelligent terminal which allows high speed control and measurement.

Configurations and features of the modules are explained. Performance of prototype modules constructed along with the design are shown. A simulation is performed by using these prototype modules.

1. Introduction

For the purpose of controlling a large number of slow response apparatus such as power supplies for magnets with a long time constant and position controllers, conventional CAMAC modules have been widely used. However, the use of many CAMAC modules is not always economical: it often increases the load of a control computer and reduces the system reliability. In order to overcome the disadvantages, we have developed two types of interfacing modules. They consist mainly of a micro-processor, memories and a communication element. The first one, CIM(Communication Interface Module), is mounted in a CAMAC crate. The second one, DIM(Device Interface Module), is placed in one or several apparatus.

They have the following intelligent functions.

- Execution of macro-programs for sequential control and data acquisition.
- 2. Periodic logging and storage of apparatus information independently of a control computer.
- 3. Block transfer of information from/to a control computer.
- 4. Automatic alarm to a control computer at an apparatus failure.

Internal Bus CAMAC Dataway > To DIM #0 Receiver / Input Transmitte Registe Selector Output CPU Register > To DIM #15 nput/ A 1-8 Output S Control RAM

Fig. 1. Configuration of CIM.

If these intelligent interfacing modules are used in a control system, the load of a control computer is reduced by the functions. Therefore, many slow response apparatus can be operated by one conventional minicomputer. Additionally, the modules ensure high speed sequential control and measurement without an aid of a control computer.

2. Configurations and Features

The configuration of a CIM is shown in Fig. 1. The CPU, ROM and RAM are commonly connected with an internal bus, which form a micro-computer. The ROM includes monitor and various task programs. The RAM stores apparatus information, and programs and data downloaded from a control computer. Information of the write data lines $W_1 \sim W_{24}$ on the CAMAC dataway is sent to the CPU, after temporarily being stored in the Input Register. Information from the CPU is sent to the read lines $R_1 \sim R_{24}$ via the Output Register. The Input/Output control generates three kinds of signals depending on the contents of F1 \sim 16 (function command), thing signals S_1 and S_2 , and a state of the CPU. The first kind of signals are control signals which allow the CPU to read/send information from/to a CAMAC equipment. The second kind of signals are status signals, Q and LAM.



Fig. 2. Configuration of DIM.

The third one is a response signal X. The Receiver/Transmitter & Selector is used for communicat ing with many DIMs by using a small number of signal wires. The CIM can link with sixteen DIM's.

Fig. 2 shows the configuration of a DIM. The DIM also includes a micro-computer. The ROM and RAM in the DIM play similar roles as those of the CIM. The Receiver/Transmitter links with the CIM through optical cables. The DIM has sixteen output ports buffered by registers and sixteen input ports with gates. These input and output ports are connected with apparatus directly or through optional components such as a D/A converter and a A/D converter. However, input ports #14 and #15 are exclusively used for fetching status information of the apparatus.

For an easy troubleshooting of apparatus, an OR-gate, a register and a flag are used. If an apparatus connected with the status input fails, the contents of the status input are varied. The resultant contents are stored in the register, which gives information to the input port #15, in response to a pulse coming from the OR-gate. At the same time, the flag is set by the pulse and sends an interrupt request signal to the CPU. After the CPU acknowledges the signal, the DIM sends apparatus failure information to the CIM. As a result, the CIM sets a LAM flag in the Input/Output control. In the troubleshooting routine of a control computer, the cause of the failure can be easily identified from the above register contents.

The DIM has a timer. In its timer task, the DIM fetches apparatus information sequentially from the input ports $\#0 \sim \#14$ at a predetermined period and stores fetched information in to the RAM. The information is sent to a control computer through the CIM in a block transfer mode.

It will be understood from the above explanation that our CIM and DIM have the following advantages over the conventional CAMAC interface modules.

i) Reduction of the load of a control computer and the overhead of the operating system.

ii) Capability of high speed sequential control and

measurement.

- iii) Enhancement of system reliability due to a reduction of the number of system components.
- iv) Reduction of the number of CAMAC equipments such as crates, crate controllers and drivers.
- ${\bf v}$) Possibility of the use of various data converters and system components with high reliability.
- Fig. 3 shows the fundamental constitution of the RIKEN SSC control system¹ with these CIM's and DIM's.

3. Performance of Prototype Modules

A CIM and a DIM according to the above mentioned configuration were constructed. CPU of them was 8051(Intel). The clock was 10MHz. Since 8051 included a timer and a function for communication, the number of components could be decreased. Communication method was asynchronous full duplex at a transmission rate of 157.5 k bits per second. The DIM had eight digital input and output ports and eight analogue input and output ports.

Experiments of testing the performance of the prototype modules were carried out with a host computer micro-11(DEC) and a CAMAC equipment including a crate controller JLSI-10 (Schlumberger).

The time required for writing data from the CAMAC dataway to an output port of the DIM and the time required for reading data from an input port of the DIM to the CAMAC dataway were measured by using the usual CAMAC commands. In a single write mode, the time was 150 μ s for one byte data and 200 μ s for two-byte data. In a single read mode, it was 230 μ s for two-byte data and 390 μ s for two byte data. In a repeat mode, the rate of data transfer between the CAMAC dataway and the DIM memory was 7 K bytes per second.

Next, a simulation of logging the response signals of controlled apparatus was done in the following manner. A function generator constituted with analogue



Fig. 3. Fundamental constitution of the RIKEN SSC control system.

Proceedings of the Tenth International Conference on Cyclotrons and their Applications, East Lansing, Michigan, USA

computation elements was used to obtain the response characteristics of controlled apparatus which could be represented by an integration system, a first order system, a second order system and a combination system of them. Block diagram of the function generator is shown in Fig. 4. The first output $V_1(t)$ is a step function voltage which comes from a digital output port of the DIM. Integrators of the same types Int 1 and Int 2 have a time constant of 400 ms. Add 1 denotes an adder. The output $V_2(t)$ was a linear sweep voltage. $V_3(t)$ and $V_4(t)$ were a quadric function and a parabolic function, respectively.

The characteristic of the circuit consisting of an inverter Inv1, an adder Add2 and an integrator Int3 was given as a first differential equation,

$$T\frac{dV_{5}(t)}{dt} + V_{5}(t) = V_{1}(t)$$
(1)

where $V_6(t) = -T \ dV_5/dt$, the time constant was 200 ms. Therefore, the outputs $V_5(t)$ and $V_6(t)$ gave different kinds of exponetial functions.

The characteristic of the circuit with an adder Add3, an inverter Inv2, and integrators of the same types Int4 and Int5 was given as a second order differential equation,

$$T^{2} \frac{d^{2}V_{7}(t)}{dt^{2}} + 2\zeta T \frac{dV_{7}(t)}{dt} + V_{7}(t) = -V_{1}(t), \qquad (2)$$

where $V_8(t) = -T \, dV_7(t)/dt$, the time constant T was 20 ms and the damping factor ζ was 0.125. Therefore, the outputs $V_7(t)$ and $V_8(t)$ were different kinds of oscillatory voltages.

The host computer could fetch each signal of the function generator through each analogue input and send out it to each analogue output of the DIM sequantially. All the output signals of the function generator could be observed at eight analogue outputs of the DIM.

Fig. 5 shows wave forms of the signals observed at analogue ports of the DIM. It is seen that wave forms(a), (b)...and (h) correspond well with output



FIg. 4. Circuit diagram of function generator used for a simulation signal logging.

signals $V_1(t)$, $V_2(t)$... and $V_8(t)$ of the function generator, respectively.

4. Conclusion

We have developed two types of interfacing modules, a CIM and a DIM, by considering the standardization of hardware, system reliability, expandability and maintenancability. A powerful control system for the RIKEN SSC will be realized by using these modules. Only seven crates are used in the control system. If conventional CAMAC interfacing modules were used in this control system, approximately thirty crates would be required. The numbers of CAMAC equipments and of wires between CAMAC crates and controlled apparatus could thus be decreased by using these intelligent interfacing modules.



Horizontal:100mS/Div. Vertical:Arbitrary Scale

Fig. 5. Output wave forms observed at the analogue output ports of DIM.

The interfacing modules may link directly with various kinds of host computers by modifying input/output control of CIM. The DIM may be utilized as a stand-alone type of instrument, e.g. a data logger, by changing its firmware.

In the asynchronous mode, the rate of data transmission between the CIM and the DIM of the prototype modules is determined by the clock frequency of CPU: max. 187.5 K bits per second. This transmission rate is not always fast. However, in a single write/read mode, the time required for data transfer between a control computer and a CAMAC dataway is long, because it depends on the performance and the operating system of a computer: 1 to 2 ms in the case of a conventional mini-computer.² Furthermore, the present interfacing modules are intelligent. Therefore, even with the above-mentioned transmission rate, controlled apparatus can be operated satisfactorily. The interfacing system is effective to reduce the number of communication from/to the control computer and enables high speed sequential control and measurement with one message from the control computer.

It will be understood that the present interfacing system is very useful for various kinds of control and measurement.

Acknowledgments

The authers wish to thank Drs. T. Sakurai and S. Motonaga for their supports. We are also indebted to Messrs Y. Nomiya and S. Katoh for their contribution to the construction of prototype modules.

References

- 1) K. Shimizu, T. Wada, J. Fujita and I. Yokoyama: RIKEN Accelerator Progress Report vol. 18(1983) to be published.
- 2) D. Burckhrt, S.Cittolin, J.O. Perersen and H. Tremlet: IEEE. Trans. Nuclear Sci. Vol. NS 28 No.5(1981) pp3845/3849.