RF - PHASE DETECTOR MODULES

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A complete new low level RF system for our cyclotron is being designed (Frequency range from 20 MHz to 40 MHz). New phase detector devices have been tested. One ECL type is developped for dee phase regulation loop, another more simple for RF cavity tunning.

1. ECL TYPE (DEE PHASE REGULATION)

We need for the phase loop, a phase detector with a linear response of $\pm \pi$ radians. Analog detectors as multiplier or RF mixer give a sinusoïdal response with a range of $\pm \frac{\pi}{2}$ radians.

Digital detectors give a linear response, but one must carefully choose the type for a good dynamic range.

For example, the monolithic ECL phase detector MC 120 40 (Fc mini 70 MHz) cannot be used because its dynamic range of $2\ \pi$ rad gives two different values for the same phase.

We develop an "exclusive OR gate" detector associated with a sense detector based on type D flip-flop.

We use fast logic (Emitter Coupled Logic). First RF signal is shaped by a diode gate device (summit 730), a line receiver (MC 1692) provides two opposite signals with ECL levels. Dual type D flip-flop (MC 1670) determines the "lead or lag" of the phase.

Nor gates (MC 1660) give signals S_1, S_2 which contains phase information in their duty cycle.

Analogic output is obtained by a low-pass filtering of S_1 and S_2 signals by an operational amplifier.

Fig. 1 shows the shematic of the ECL phase detector.
Fig. 2 shows different signals and their relationship.
Fig. 3 is the bloc diagram of the diagram of the complete phase detector.

For a good accuracy, it will be necessary to have a constant level on the ECL phase detector.
A simple automatic gain control allows a wide dynamic input level.

- Digital phase detector gives a constant output sensitivity (S = 50 mV/d°) for a frequency up to 50 MHz and a phase variation of $\pm \pi$ radians.

- Its bandwith is controlled by the low-pass filtering amplifier.

- The design requires R.F. technics (Pc board with ground planes, capacitive feedthrought for supplies, shielding box, matched delays).

- This phase detector accepts a wide dynamic amplitude variation of the input RF signal (more than 30 dB for less 1 % of phase error).

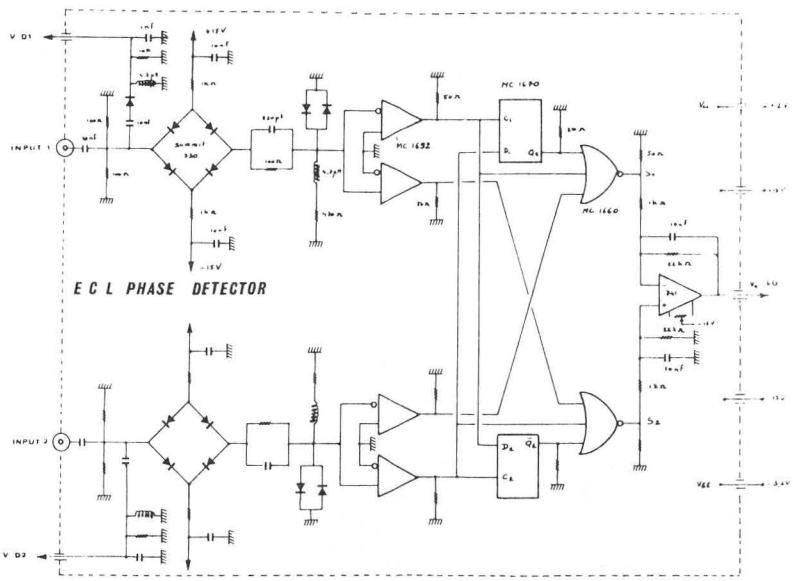


Figure 1

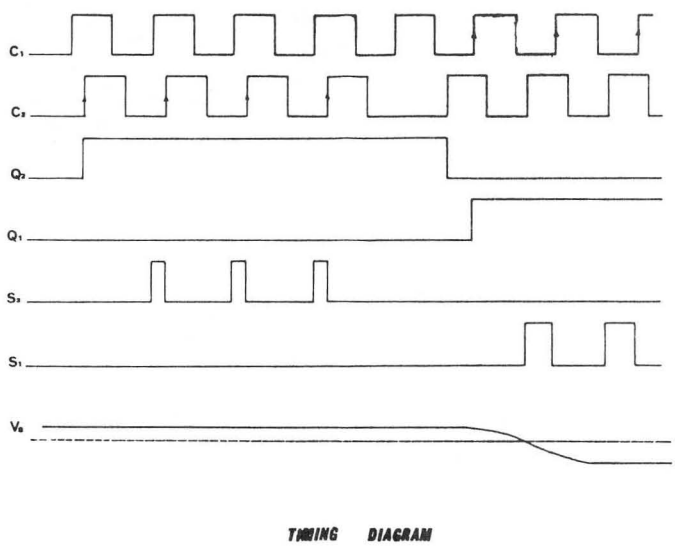


Figure 2

2. D.B.M. TYPE (CAVITY TUNNING)

The main part element in the automatic cavity tunning loop is the phase detector. We have developped one with a 18 dB dynamic input and 20-40 MHz frequency range. Sinus and cosinus phase analog outputs are performed to provide a modulated signal compatible with the stepping motor translators.

Automatic tunning loop synoptic (Fig. 4)

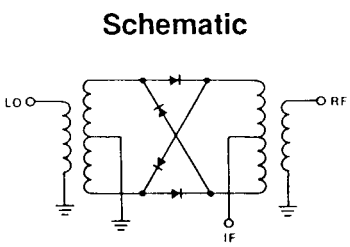
- When the cavity is correctly tunned, the phase between plate and grid voltages is 180 degrees, the detector output voltage must then be zero.

- Phase detector must accept amplitude variation on its inputs (grid and plate voltages can swing up to 20 dB).

- The phase response must also be independant from the frequency in the 20-40 MHz range.

- The reliability and long term stability are necessary.

For all these reasons we used a double balanced mixer (D.B.M.) optimised as phase detector (mini circuit RPD-1). When a D.B.M. works on phase detector it is a particular case of mixing. When W_{Lo} and RF input signals are at the same frequency.



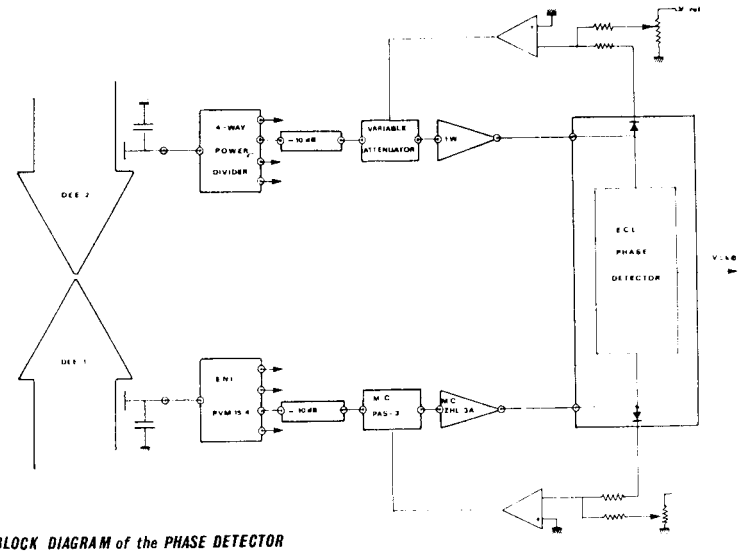
The mixer equation is :

$$If = A_1\cos[(W_{Lo} - W_{RF})t - (\phi_{Lo} - \phi_{RF})] + A_2\cos[(W_{Lo} + W_{RF})t + (\phi_{Lo} + \phi_{RF})] + \text{higher order terms.}$$

if $W_{Lo} = W_{RF}$ and after low pass filter.

$$IF = A_1\cos(\phi_{RF} - \phi_{Lo}).$$

The response depends on the cosinus of the phase difference between Lo and RF inputs as well as on signal amplitudes.



BLOCK DIAGRAM of the PHASE DETECTOR

Figure 3

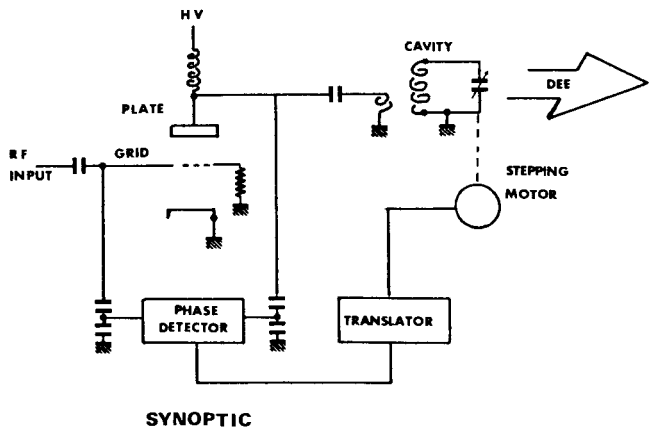


Figure 4

REALISATION (Fig. 5)

For our application, a 90° phase shift is necessary to achieve the sinus of the phase difference. We obtained this by using a quadrature hybrid junction (ANZAC JH 114), a second identical junction used in zero phase to compensate the phase shift error versus of frequency.

To minimize amplitude input signal errors, the D.B.M. works at a nominal constant level (+ 7 DBM). A simple amplitude regulation is performed on each input. The sinus DC phase voltage is used as error signal in the tunning loop. The cosinus signal after triggering gives validation for sinus output.

Fig. 6 shows sin ϕ = fs (frequency) Fig. 7 shows sin ϕ = fs (amplitude).

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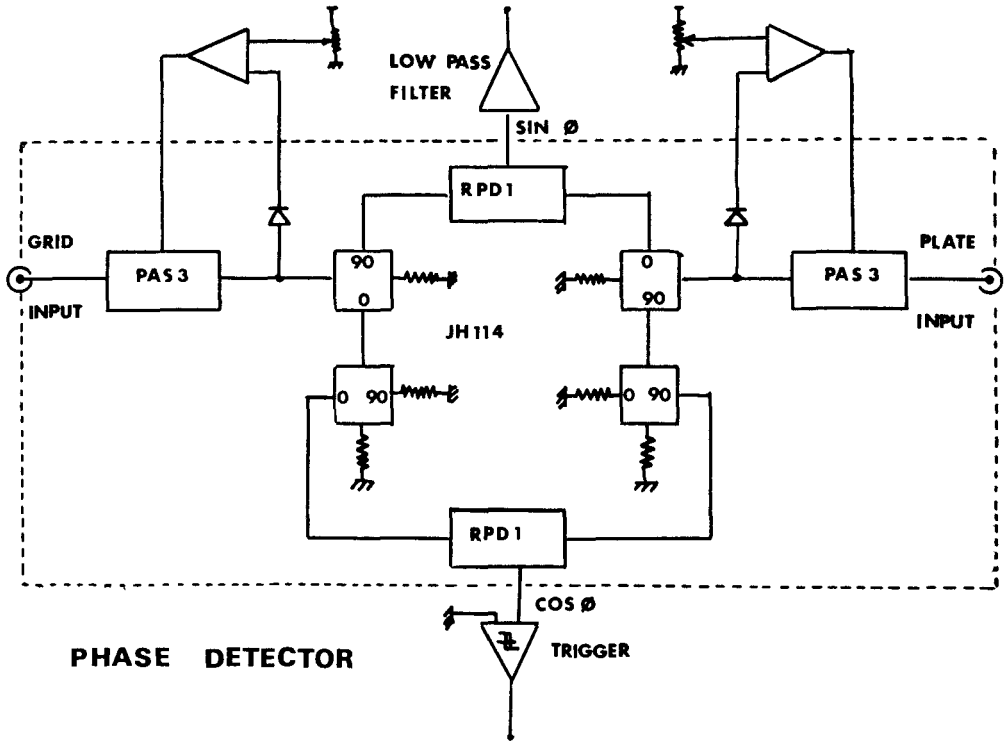

Figure 5

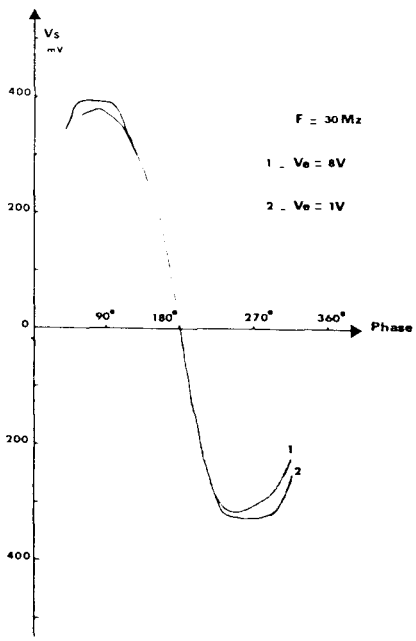

Figure 6

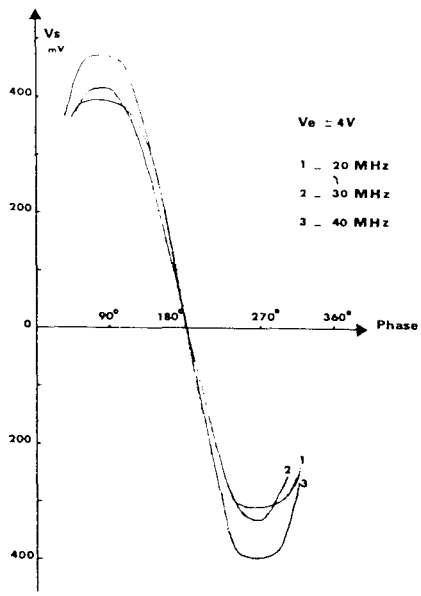

Figure 7

3. CONCLUSION

The first type is more sophisticated and more performant.

The second type is enough for RF cavity tunning. It is not expensive and easy to build.

REFERENCES

- P. K SIGG SIN NIM 187 (1981) Beam phase stabilisation.
- GANIL RF SYSTEMS. B. DUCOUDRET, A. JOUBERT, F. LABUSSIERE.
- Motorola notice and datasheets on ECL components.
- RTC notice on ECL design.
- S. GASNIER CNRS, Service du Cyclotron Orléans, 1979. Internal Report.
- ANZAC notices.
- Minicircuit notice on phase detector.