UTILIZING MULTIPLIER STACK'S REFLECTED PARASITIC CAPACITANCE TO ACHIEVE ZVS OPERATION OF RESONANT INVERTER FOR 750 keV DC ACCELERATOR

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Abstract

This paper presents the analysis and design of a high order LCLC resonant inverter that uses the reflected capacitance of the Cockcroft-Walton based multiplier stack as its tank circuit component. The inverter is being used for energizing the HV generator of the 750 keV dc accelerator developed at RRCAT, Indore. High frequency resonant inverters are replacing the conventional PWM counterparts due to high efficiency, reduced size, weight and cost. The operating characteristics and analysis of series resonant (SRC), parallel resonant (PRC) and series parallel (SPRC) resonant converters have been reported for fixed frequency operation. It has been shown that SPRC takes the advantage of both SRC and PRC curtailing their disadvantages. The inverter described feeds a high frequency, high voltage (HV) transformer isolation and utilizes the otherwise unwanted parasitic components to its advantage.

INTRODUCTION

Hard switching PWM inverters for high voltage application need to feed a very high voltage transformer. The HV transformer requires a relatively large spacing between the primary and secondary windings, which leads to a relatively large leakage inductance. In this case, it is generally difficult to employ a PWM type inverter due to output voltage lost during the reversal of current in the large leakage inductance of a high voltage transformer. On the other hand, an operating frequency higher than 30 KHZ is generally desired to avoid voltage drop across the capacitive column of the high voltage multiplier stack and to avoid any audio frequency noise that may be generated. This in turn improves the load regulation of the system. But it also enhances the effect of parasitic components. A sinusoidal voltage is desired as high frequency harmonics in the square wave voltage impose high dv/dt stress. For lower switching losses, high power density, better EMI characteristics and sinusoidal voltage and currents, resonant inverters have proved to be a better proposition. A series resonant inverter has the disadvantage of high circulating currents that increases the switching device ratings. Furthermore, a series resonant inverter cannot actually be developed due to the large parasitic capacitance generally existing in a high voltage transformer. Hence a series parallel LCLC combination has been used as it gives the advantage of low device currents and a better load regulation. The converter utilizes the leakage inductance and the inter-winding capacitance of the high voltage transformer it feeds to and the parasitic capacitance of the multiplier stack, for its resonant operation. This LCLC resonant tank functions to position zero voltage across the switching device prior to turn on, eliminating any power loss due to the simultaneous overlap of switch current and voltage at each transition.

The multiplier stack basically consists of several similar circuits containing diodes and capacitors, which are connected in series to achieve voltage multiplication. The high voltage rating demands the placement of components to be fairly apart to achieve required voltage isolation. The circuit is fed with a 40 kHz sine wave to achieve better regulation and minimum ripple at the DC output. Combined together, all these results in higher parasitic components. These capacitances are mostly contributed by parasitic capacitance between DC and AC columns of multiplier stack, diode capacitance etc. Moreover the stack is fed from a 45 kV-0-45 kV high voltage transformer with a very high step-up ratio, which is 150 in our case. The transformer secondary itself imposes high distributed capacitance

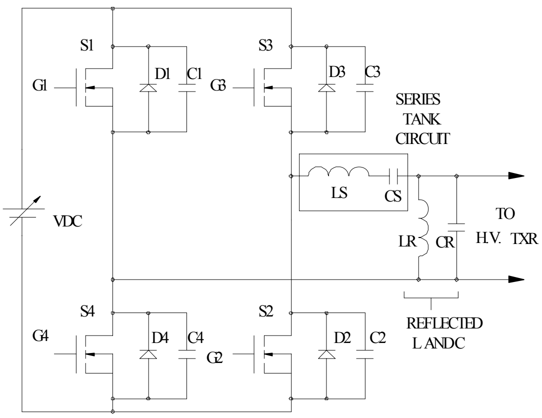

Figure 1: High frequency inverter.

OPERATION

When measured at the primary of the HV Transformer with the multiplier stack connected at its secondary, the reflected load at inverter output was found to be purely capacitive with a value of 4.1 μF. This could have been compensated by a parallel inductance on the primary side but it would have then resulted in high circulating currents in the transformer winding. Referred to the secondary side of the transformer, this capacitive reflection effectively comes out to be 0.177 nF.

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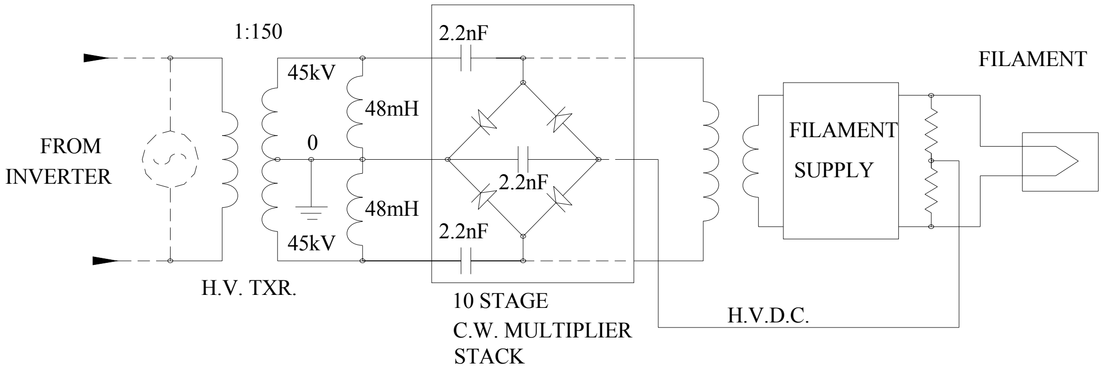

Figure 2: High voltage generator.

The compensating inductance required then was 96 mH to keep the resonating frequency very close to switching frequency of 40 kHz. This selection kept the no load circulating current demand at the switch end to the minimum possible.

A full bridge topology with fixed frequency operation is used in this inverter. The diagonal switches are driven together alternately to place an AC voltage across the resonant tank. Power is only transferred to the output section during the ON times of the switches. When the switch pair, which is currently on is switched off the primary current flows into the switch output capacitance causing the switch drain voltage to resonate to the opposite input rail. At the same time a current flows the output capacitance of the other pair of the switch discharging it to zero voltage enabling Zero Voltage Switching upon its turn on. An intentional dead time has been introduced in the power conversion cycle by using a higher value of resonant inductor, whereby the switch remains off and is clamped at zero voltage by the resonant tank. Rather than turn on the switch instantly when the zero voltage is attained, the switch is held off while the primary current circulates through the body diode. This has been done to achieve the ZVS condition for the full range of operation of the inverter. The minimum time available for the charged snubber capacitor placed across the off device was found to be 1.56 µS, under worst case of no load condition. The resonant inductive energy was sufficient to discharge the capacitor before the device was put on thus ensuring the ZVS operation.

The inverter output is varied by varying the input DC, which is tapped from a fully controlled 3-phase rectifier. The switching devices used are Mitsubishi make half bridge IGBT modules (CM200DY-24H). The switching frequency is kept at 40 KHZ. The series LC is tuned at 40 KHZ, which filters the higher harmonics to yield sinusoidal fundamental of 40 KHZ at the output. The parallel LC tank is tuned at 45 KHZ to limit the circulating current to 20% of the full load current at no load condition. This though impresses higher stress on switching devices, it yields the desired load regulation. The inverter operates under ZVS for the complete range of load variation. Thus a loss less snubber containing only a capacitor of 10 nF across each device has been used. This further improves the power transfer efficiency of the inverter. Complete discharge of the snubber capacitor has been assured under the worst case of no load condition to ensure ZVS operation of the inverter. The driver card designed for the switching device blocks the firing pulses in case the capacitor is not completely discharged by the load current avoiding lossy turn on of the device. The inbuilt anti-parallel diode of the IGBT module has been used to provide path for the freewheeling current.

CONCLUSION

The inverter has been tested up to 25 KW by using a water load and all the waveform have been found to be as stipulated. This inverter feeds a center tapped high voltage transformer with secondary peak voltage rating of 45kV-0-45KV. The transformer in turn feeds a 10-stage symmetrical voltage multiplier stack to generate the required DC high voltage of -750 kV.

REFERENCES

[1] J. R. Pinheiro, T. F. Pegoraro and J. E. Baggio, “Analysis and design of a DC/DC ZVS PWM off-line converter”, IEEE Applied Power Electronics Conference (APEC), 1998, pp.640-645.

[2] A. K. Bhat and V. Belaguli, “Analysis and design of hybrid parallel-series resonant converter” IEEE Trans. Circuits and Systems, Part-I: Fundamental Theory and Applications. Vol. 44, No. 8, Aug. 1997, pp. 705-711.