HEAT DISTRIBUTION ANALYSIS OF PLANAR BALUNS FOR 1KW
SOLID-STATE AMPLIFIERS AND POWER COMBINING FOR 1.8KW

Tsung-Chi Yu, Chaoen Wang, Lung-Hai Chang, Meng-Shu Yeh, Ming-Chyuan Lin, Tz-Te Yang, Fu-Tsai Chung, Yu-Han Lin, Ming-Hsun Tsai, Mei-Hsia Chang, Chih-Hung Lo, Ling-Jhen Chen, Zong-Kai Liu, NSRRC, Hsinchu, Taiwan

Solid-state transmitter for booster and storage ring in synchrotron would be composed of hundreds of amplifier modules. The amplifier module is biased at class AB and constructed in push-pull operation. Recent trend of amplifier module design features higher power up to 800 Watts and equipped planar balun (balance-unbalance converter) for push-pull operation. In NSRRC, the exclusive round planar design has encountered high temperature situation at kW range. Therefore, further study on this thermal condition is carried out in this study. Four types of planar balun design and two laminate materials are used for heat analysis. The typical coaxial balun is also applied on actual amplifier design. The results bring the better design with proper laminate choice and leads to acceptable thermal distribution with 1kW output power at 500MHz. Besides, for a more compact module with higher output power, the combination of two chips on the same circuit reaching 1.8kW is also presented.

Four Planar baluns for heat analysis

Figure 1: Four version planar baluns layout for power amplifier application

Figure 2: (a-c) The developed planar balun integrating on circuit boards (d) the coaxial balun used as reference

High power thermal tests

Figure 3: (a, c) The black paint* covered planar balun and coaxial balun amplifier circuits for heat analysis during high power operation as (b, d) *the black paint can have uniform emissivity of 0.95 over circuit surface

Figure 4: (a) thermal distribution of uncovered chip during high power operation (b) the chip temperature will decrease after output power of 500W

Figure 5: (a) the maximum temperature of various version planar balun by sweeping output power (<200°C) (b) the efficiency of the tested circuits

Dual-chip combination within one module

Figure 6: (a) Power gain of the tested circuits (b) Thermal stability duration test of the developed circuits from zero to full power

Figure 7: (a) the dual-chip circuit by Gysei power combiner(b) the IR image of dual-chip combination circuit

Separate test results of two chips

Figure 8: (a) drive power vs. output power, (b) output power vs. power gain (c) power gain vs. power gain and (d) output power vs. power gain of these two chips on the same module

Power combination of dual-chip

Figure 9: (a) maximum power of 1800W is derived (limited by drive power) (b) power added efficiency vs. output power of the dual chip combination circuit

Power gain versus (a) drive power and (b) output power

Figure 10: power gain versus (a) drive power and (b) output power

Long-term reliability test of the dual-chip circuit

Figure 11: (a) 43 days (1032 hours) long term reliability test of the dual chip circuit (b) The efficiency dropping about 2.5% may result from the dry of thermal conducting grease