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DEVELOPMENT AND CONSTRUCTION STATUS OF NEW LLRF CONTROL SYSTEM FOR SUPERKEKB

T. Kobayashi#, K. Akai, K. Ebihara, A. Kabe, K. Nakanishi, M. Nishiwaki, J. Odagiri,
KEK, Tsukuba, Ibaraki, Japan
H. Deguchi, K. Hayashi, T. Iwaki, M. Ryoshi,
Mitsubishi Electric TOKKI System Corporation, Amagasaki, Hyogo, Japan

Abstract

Beam commissioning of the SuperKEKB will be started in 2015. A new LLRF control system, which is an FPGA-based digital RF feedback (FB) control system on the MicroTCA platform, has been developed to satisfy the requirement for high current beam operation of the SuperKEKB. The good performance of the prototype was demonstrated in the high power test with an ARES cavity. Then the quantity production with some refinements is in progress. As a new function, klystron phase lock loop was additionally implemented within the cavity FB control loop in the FPGA, and it was successfully worked in the low-level operation test.

In this report, the latest design and new progress of the LLRF control system are summarized including the RF reference distribution system.

INTRODUCTION

SuperKEKB is a new upgrade project, which is aiming at 40-times higher luminosity than the KEKB [1], accordingly it requires much lower-emittance and higher-current beam storage. Accuracy and flexibility in accelerating field control are very essential for storage of high-current and high-quality beam without instability.

A new low level RF (LLRF) control system, which is based on recent digital architecture, was developed for the SuperKEKB, and the good performance of the prototype was demonstrated in the high power test as reported in Ref. [2]. After some refinements, the quantity production was started last year. The progresses of the production and installation are now on schedule. The existing analogue LLRF systems used for KEKB operation will be replaced by new ones, step by step.

The accelerating frequency of the storage ring is about 508.9 MHz (CW operation). The regulation stability of 0.02% and 0.02º (rms) in the cavity amplitude and phase, respectively, were obtained in the high power test of the LLRF control system [2]; that sufficiently satisfies the requirements.

For the beam acceleration, both normal conducting cavities (NCC) and superconducting cavities (SCC) are used. The NCC, which is called ARES [3], has a unique structure for the KEKB in order to avoid the coupled-bunch instability [4]. ARES is a three-cavity system: the accelerating (A-) cavity is coupled with a storage (S-) cavity via a coupling cavity.

A damping ring (DR) will be constructed at the injection linac for the positron emittance reduction. In the DR, the RF-frequency is the same as that of the main ring (MR), and three cavities, each of which is a HOM-damped single cell cavity (not an ARES type), are driven by one klystron for the acceleration. Thus another LLRF control system for the DR was also designed. It is almost the same as that of the MR, except the three-cavity vector sum control is required.

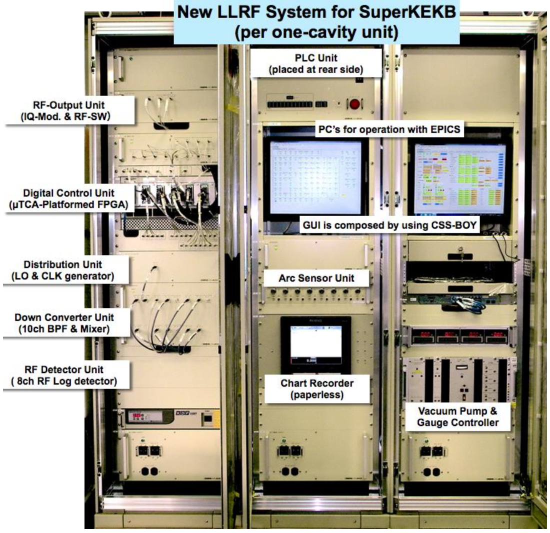

Figure 1: LLRF control system for SuperKEKB.

NEW LLRF SYSTEM FOR SUPERKEKB

Figure 1 shows a picture of a mass-production model of the new LLRF system for the SuperKEKB. A block diagram of an ARES cavity driving system is shown Fig. 2. One klystron drives one cavity unit, so one LLRF control system corresponds to one cavity-unit control.

In the digital control unit (Fig. 1), five FPGA boards function as MicroTCA-standard advanced mezzanine cards (AMCs) [2][5]: Digital FB Controller (DFBCNT), Tuner Controller (TNRCNT), Inter-Lock Controller (INTLCNT), RF-Detector Monitor (RFDETMON) and Arc-discharge Monitor (ARCMON). The DFBCNT, TNRCNT and INTLCNT have 4-channel 16-bit ADCs and DACs [5]. RFDETMON and ARCMON have 8-channel 14-bit ADCs. For slow interlocks (e.g. vacuum, cooling water) and sequence control, a PLC is utilized. EPICS-IOC on Linux -OS is embedded in each of the FPGA boards and the PLC [6].

Monitoring RF signals are down-converted into 10-MHz IF signals, and then I/Q-sampled by ADCs at the FPGA boards. Proportional-integral (PI) FB control is applied to the vector modulation by the DFBCNT. The "μ

#tetsuya.kobayashi@kek.jp

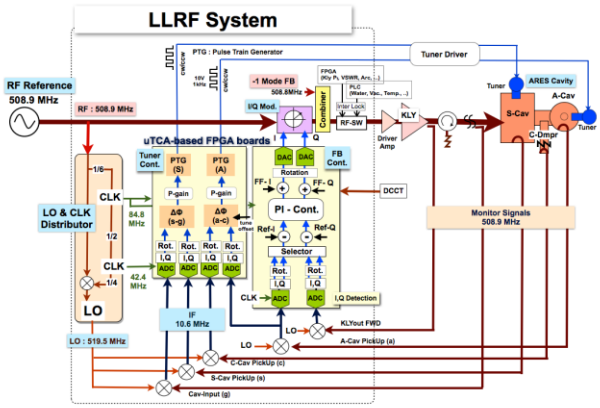

Figure 2: Block diagram for ARES cavity control.

= -1 mode" control signal can be combined with driving-output for suppression of coupled bunch instability [4].

For ARES cavity, two tuners of S-cavity and A-cavity are controlled concurrently by the TNRCNT. Besides piezo tuner controller is implemented in the FPGA for SC cavity; it generates analog voltage output for the piezo control.

The INTLCNT monitors cavity reflection and the VSWR, and it also summarizes all of the other FPGA's interlock states to switch RF-off. The RFDETMON acquires waveforms of RF log detectors at 42.4 MS/s like an oscilloscope, which makes flexible filtering or discrimination possible for the interlock. External trigger is also available for the acquisition. Similarly, the ARCMON also acquires photo-signals detected by the arc-sensor unit (Fig. 1) which has 8-channel photo sensors to detect discharge in cavity input coupler, klystron window and circulator. The photo sensor is a high-speed photomultiplier-tube (Hamamatsu Photonics H10721). Large-core optical fibers are used to transfer the discharging flashlight to the arc-sensor unit. The performance of the arc-sensor with the large-core fiber was evaluated, then sufficient sensitivity and responsive property were verified for the arc-detection [7].

For the mass-production, several refinements from the prototype were applied to the FPGAs; for example, mini-size loose coaxial connectors on the front panel were changed to bundled type by a fixed connector, and also the clock distribution was improved to be lower jitter. Furthermore, the FPGA board was upgraded to be possible to remote-update the configuration program (firmware), so the FPGA firmware of all stations can be updated remotely concurrently.

PRODUCTION AND INSTALLATION STATUS OF THE LLRF

Figure 3 shows the RF system configuration for the SuperKEKB, laying about thirty klystron (LLRF) stations in the MR. In the beginning of the commissioning, the new LLRF systems will be applied to nine stations for the ARES cavities at the OHO section as shown in Fig. 3. The quantity production of the new eight systems was accomplished, and the installation and the system tuning are just in progress. Additional one system will be produced in this fiscal year. The other stations will be operated with existing analogue systems in the first commissioning. The DR-LLRF installation and operation is scheduled in next fiscal year.

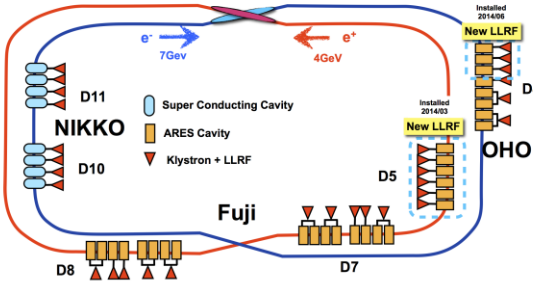

Figure 3: RF system layout for the SuperKEKB. Nine LLRF stations are replaced with the new ones.

KLYSTRON PHASE LOCK LOOP

As reported in the previous IPAC, 80-deg. phase shift in a klystron output was observed in the high power test [2]. This phase shift is the result of the anode voltage control depending on input power to optimize the collector loss for the efficiency, and it is unexpectedly large. The phase shift (or I-Q coupling) inside the closed loop makes I/Q-FB control unstable. According to our estimation, acceptable phase shift is within +/-50 degrees in our operation condition.

For the above reason, additional function of klystron phase lock loop (KLY-PLL) was implemented into the DFBCNT as shown in Fig. 4. It works digitally in the FPGA with the cavity-FB control. Additional phase-rotation function is inserted before the DAC outputs to the I/Q modulator to cancel the phase shift. The required loop bandwidth for the KLY-PLL is supposed to be less than 1 kHz, because the anode voltage control response is approximately 1 Hz.

Figure 5 shows test results of the KLY-PLL with an ARES cavity. In this test, the ARES cavity was driven by a 100-W driver amplifier without klystron, so it is not high-power test. A voltage-controlled phase shifter was inserted in the loop, and it rotated the phase by 90 degrees at 1 Hz as shown in the figure; the green line indicates the

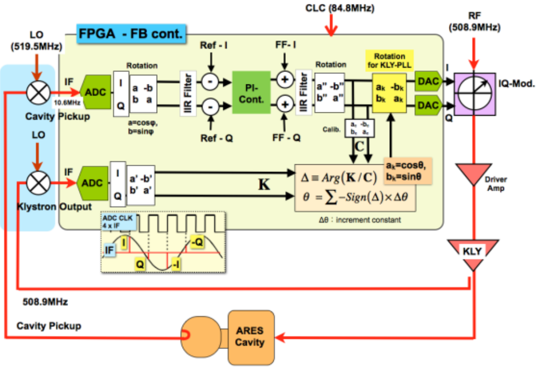

Figure 4: Block diagram of FB control and klystron phase lock loop in the DFBCNT.

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phase shift, while the orange line is the cavity pick-up phase under cavity FB-control. As shown in the figure, the KLY-PLL worked well as expected, and consequently cavity FB control was still stable.

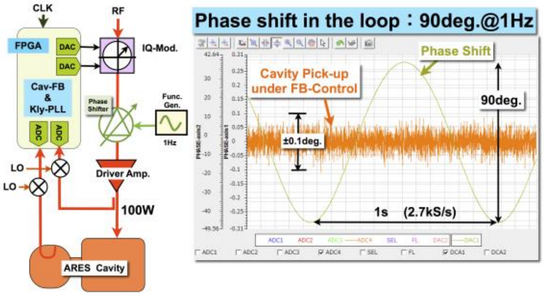

Figure 5: KLY-PLL test result with an ARES cavity by 100-W driving.

RF REFERENCE DISTRIBUTION

RF reference distribution system was also newly designed for SuperKEKB. The require phase stability for the RF reference is ±0.1 degrees (pk-pk) during beam operation. The RF reference signal of 508.9 MHz is optically divided and distributed into six RF sections, the damping ring and the Belle-II detector from the central control room (CCR) by means of “Star”-topology configuration with the “Phase Stabilized Optical Fiber (PSOF)”. The installation of the PSOF cables in the accelerator tunnel was already completed.

Furthermore, for the thermal drift compensation of the multi-divided optical transfer lines, a multiple optical delay control system was developed as shown Fig. 6. MTCA-AMCs (FPGA boards) monitor the phases of respective round-trip signals by direct-sampling method, and they control respectively variable optical delay lines (VODLs) to cancel the phase change. With this VODL control system, the required phase stability of ±0.1 deg. was completely achieved [8]. Figure 7 shows the picture of the VODLs for eight distributions and the multiple VODL control system (MTCA-AMCs), which was already installed at the CCR.

The E/O and O/E used in this system are the same as that for the J-PARC Linac [9], which are equipped with Pertier device for thermal stabilization. The transfer jitter with them is 110 fs (rms) as the measured result.

SUMMARY

For the SuperKEKB, a new LLRF control system, composed of MTCA-platformed FPGA boards with embedded EPICS-IOC, has been developed. After many refinements applied, now the mas-production and installation are in progress. Before the commissioning start, nine LLRF stations among existing thirty stations will be replaced with the new ones.

Klystron-phase lock function was implemented into the FPGA in order to cancel the large klystron phase shift of 80 degrees due to the efficiency optimization. It worked successfully with an ARES cavity in 100-W driving test.

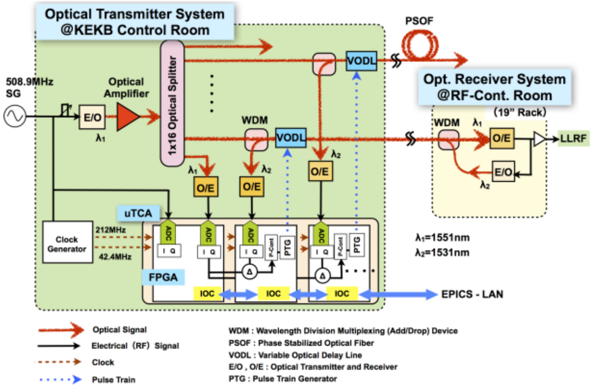

Figure 6: Functional block diagram of the reference distribution system with thermal drift compensation.

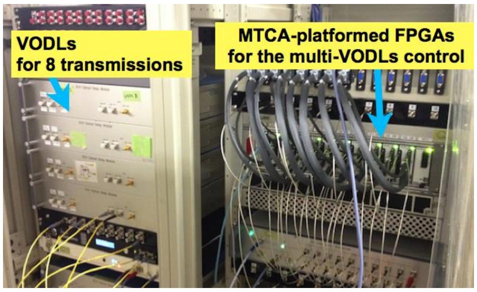

Figure 7: Picture of the multiple VODL control system installed at the CCR for the stabilization of the RF reference distribution.

RF reference distribution and stabilization system will be also upgraded to be Star-topology optical distribution for eight destinations from the CCR with the PSOF cables installed in the acc. tunnel. The phase stability of ±0.1 (pk-pk) deg. is realized with the multiple VODL control system by using FPGAs.

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