MITIGATING NOISE SOURCES IN MTCA.4 ELECTRONICS FOR HIGH PRECISION MEASUREMENTS*

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Abstract

The RF field detection instrumentation plays a crucial role in modern accelerator performance. The most critical section is the transition from the analog signal processing to the digitalization. In this paper we present state of the art performance of COTS components and limitations imposed by crate-oriented solutions. We give recipes on how to optimize performance and present some of the recent results.

INTRODUCTION

When it comes to high-end instrumentation, proper design of analog and mixed signal processing circuits (ADCs and front-ends) plays a key role. Same applies for instrumentation in the MTCA.4 form factor where the expected output dynamic range of the processed signal is better than >90 dBFS at 40 MHz bandwidth (with no filtering). A standard MTCA.4 module is a PCB of roughly 200 mm x 140 mm in size. These are usually more than 6 layer modules with RF inputs in the rear side and the digital outputs leaving in the front side over an AMC backplane [1]. The connectivity of such units between front and back is achieved over Zone 3 ERNI ADF [2] connectors (ERmetZD-10x3P-FEM).

Disturbances that reduce the dynamic range of the signal can originate outside the board or can be generated on the board where they are being measured. Assuming that the proper operating point of components has been achieved, the disturbances generated externally can be mitigated by proper shielding (magnetic/electrical) and GND structure (rack/crate/AMC+RTM) if radiated. Proper GND structure helps mitigating also conductive disturbances that are located on the signal/power pins since inhomogeneous GND that is distributed over the system represent a possible threat.

The former is a very common source of problems in distributed systems if not addressed properly since the connectivity between dislocated units is needed and these usually don't have tightly connected GNDs. One possible approach is to use differential signals or optical interconnections. The focus of the paper will be on disturbances generated on the board.

COUPLING MECHANISM

In the paper we assume that in a classical front-end + ADC architecture the noise floor is defined by the ADC. The amplitude close-in distribution is defined by the coupling of phase noise to amplitude noise. Close-in phase noise performance is defined by the residuum phase noise

of the subtraction of REF-LO-CLK (mixers and dividers) and the residual contribution of the sampling circuit in the ADC.

The basic mechanism of coupling of disturbances follows the idea that potential differences between various locations on the PCB or between interconnected modules will cause GND currents which effectively means that disturbances can be measured on the signal of interest A non-zero impedance R between the source and the circuit induces an additional voltage in front of the circuit which convolutes with the input RF signal V0. In the simplest case the disturbances are only superimposed and in the extreme cases they are nonlinearly modulated with the signal of interest. The mechanism of current-sharing is depicted in Fig. 1

A simplifying circumstance is the fact that the signal of interest might be shifted in frequency or in time compared to the disturbance. In this case problems can still be avoided by using a higher frequency carrier which shifts the processing frequency to a band where the disturbances are clearly separated from the main signal and by proper filtering they can be removed.

The basic model of such coupling mechanism of the disturbance to the signal of interest (V0) is shown in Fig.1. The example described above assumes that function f is a simple addition.
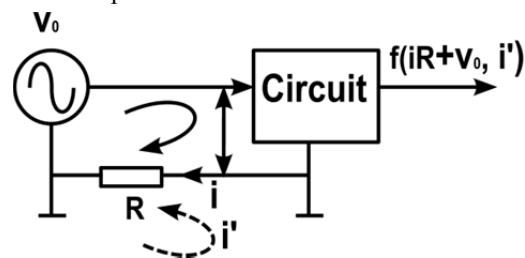

Figure 1: Principle of coupling of disturbances.

The usage of a frequency translation or time translation cannot help if the coupling of disturbances follows a more complex equation (e.g. modulation). This will likely cause an amplitude and phase modulation of the main signal with the disturbance.

Mitigation

One possible way to avoid such effects is a proper placement of components on the PCB. This will prevent currents originating from different devices to share the same grounds. Predicting current flows on a multilayer PCB is a complex problem and it can be mainly studied via RF/Microwave simulation tools.

If the problem of "current-guiding" becomes to involving a common engineering practice suggests to make one

solid GND over the whole PCB. In this case the goal is to minimize R (see Fig. 1) as much as possible by means of parallelism of structures (e.g. GND planes, power planes, shields, vias etc.) that might include some residual ohmic resistance. Both approaches have disadvantages and advantages and are frequently used in modern PCB designs.

TEST SETUP

The guidelines described above are just the basics of proper low-noise designs. One of the efforts and its results toward a spurious free design is shown in Fig.2-3. Integrated jitter of 5 fs phase and 6e-6 amplitude uncertainty at 1.3 GHz ([100 Hz – 40 MHz]) corresponds to the integrated jitter over the given bandwidths.
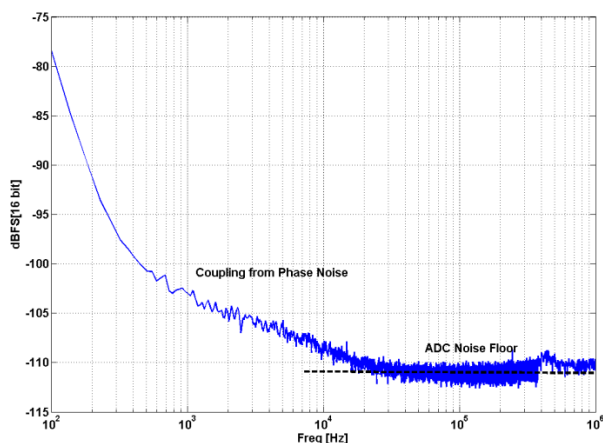

Figure 2: Measured amp close-in spectrum over the first Nyquist zone. Sampling frequency is 81.25 MSPS, N = 16384 samples. The IF sampled frequency is 54 MHz.
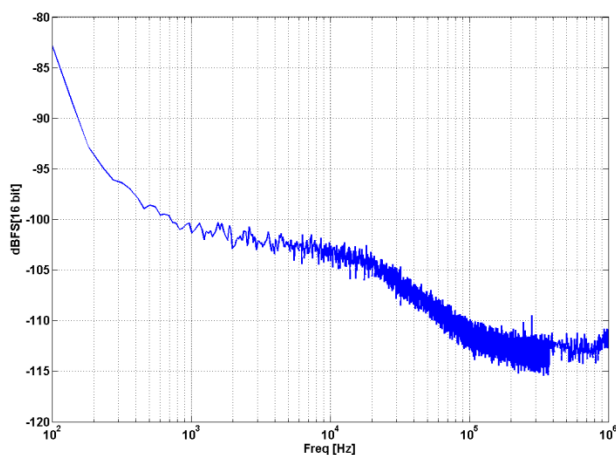

Figure 3: Measured phase close-in spectrum over the first Nyquist zone. Sampling frequency is 81.25 MSPS, N = 16384 samples. The IF sampled frequency is 54 MHz.

The measurements presented in Fig.2 and 3 were done by feeding the same reference signals as is used for generating the CLK and LO signals to the down-converter channel. The processing algorithm in the FPGA includes several parallel decimating filters which extend the resolution of the FFT. A simplified block diagram is shown in Fig. 4..
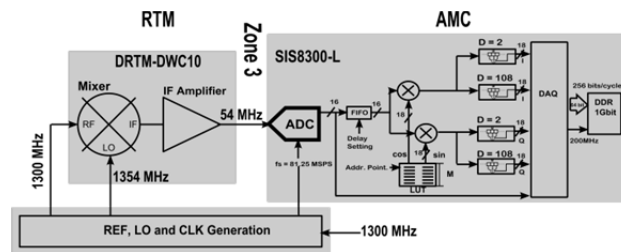

Figure 4: Block diagram of the test setup.

SUMMARY

Instrumentation build into compact and modular platforms requires specific expertise for mitigating disturbance. In the paper we have focused on a specific problem (coupling mechanism of disturbances on the signal) and explained its mechanism. An example has been presented that summarizes all the recommendations put in practice. Results show that as low as 4 fs and 6e-6 phase and amplitude uncertainties ([100H-40 MHz]) can be achieved.

ACKNOWLEDGEMENTS

REFERENCES

[1] http://www.picmg.org/
[2] http://www.erni.com/