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DESIGN, IMPLEMENTATION AND PRELIMINARY TEST RESULTS OF THE ESS BEAM CURRENT MONITOR SYSTEM

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Abstract

The Beam Current Monitor system of the ESS linac will be mainly based on AC Current Transformers. The BCM system will be used to monitor the beam current and charge in absolute and differential modes. The differential current measurement is also intended for detecting large and sudden beam losses and acting on the Machine Interlock System (MIS), especially in areas where Beam Loss Monitors cannot be reliably used. A demo BCM based on a Bergoz ACCT and MTCA.4 electronics has been procured and integrated into EPICS. A VHDL code has been developed and successfully tested for the required FPGA signal processing including droop compensation, filtering, DC level correction and interfacing to the MIS. This paper gives an overview of the current status of the BCM system design and implementation as well as some preliminary test results in absolute and differential modes.

INTRODUCTION

The Beam Current Monitor (BCM) system of the ESS linac will be used to measure the beam current and charge in absolute and differential modes in addition to providing fast inputs to the Machine Interlock System (MIS). The BCM system will consists of 20 AC Current Transformers (ACCTs) approximately, and one or two Fast Current Transformers (FCTs). There will be a higher concentration of ACCTs in the low-energy linac, so that they can be used as a substitute to the Beam Loss Monitor (BLM) system to shut the beam off in case of a fast beam loss, thus avoiding potential damages to the linac components. The FCT(s) will be mainly used to measure the performance of the Medium Energy Beam Transport (MEBT) chopper with a rise time of 10 ns app.

It is planned to use commercial off-the-shelf ACCT sensors and connect them to some front-end electronics that will be partly custom designed. The digitizer card will be procured externally, but the FPGA code will be done in-house. MTCA.4 has so far been used for the ACCT prototyping and test. A decision for the final electronics platform is expected in the second half of 2014.

The top-level parameters of the BCM system and some preliminary test results are presented in [1]. In this paper, the focus will be on the recent progress in the areas of FPGA signal processing, interfacing to the MIS, ACCT signal transmission and ACCT tests result in the presence of an external magnetic field.

BCM DESIGN OVERVIEW

Figure 1 shows a simplified block diagram of a potential solution for the final ACCT implementation.

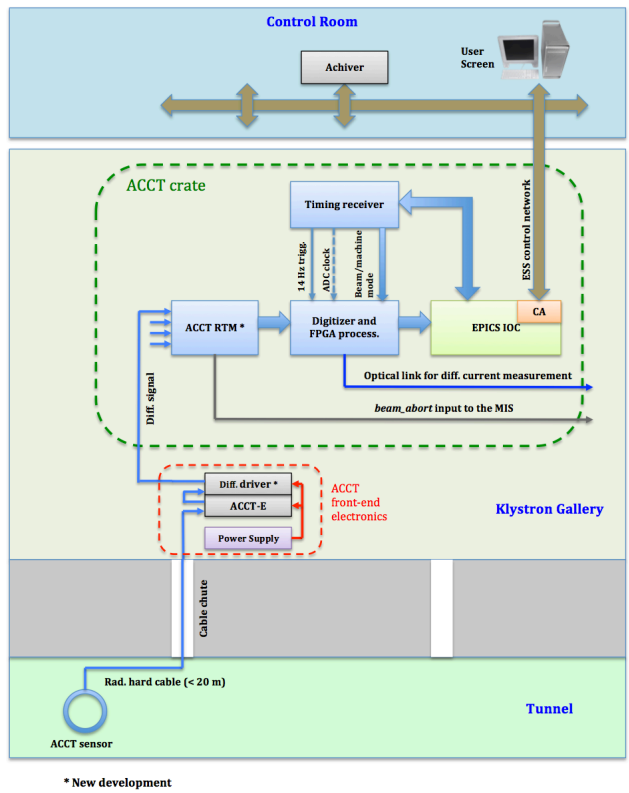

Figure 1: Simplified block diagram of the ACCT system.

A radiation-hardened cable with a length of 20 m (max) should be used to transfer the ACCT signal from the tunnel to the front-end electronics (i.e. the ACCT-E module in Fig. 1) in the Klystron gallery. Longer cables will result in a ringing or a longer response time as well as a higher noise level. A differential driver sitting next to the ACCT-E module will convert its output signal to differential with the advantage of rejecting the common-mode noise. This signal will then be sent over a shielded cable to the ACCT Rear Transition Module (RTM) hosted by the MTCA.4 crate. The RTM will receive the ACCT signal in a differential format and after some minor signal

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conditioning, send it to the digitizer card where it will be sampled and FPGA processed. The differential driver and the RTM will be designed so that they match the impedance and the dynamic range of the front-end electronics to the digitizer input. The digitizer card will receive timing signals and beam/machine mode data from a timing receiver card sitting in the same crate. The resultant ACCT data will then be communicated to the user interface through the EPICS IOC and Channel Access. An optical link will provide a fast data communication channel to transfer the ACCT data from one digitizer card to another if needed for the differential interlock.

The current setup follows the same design concept, but the differential driver, the ACCT RTM and the optical link are not available yet.

The data acquisition electronics of the FCT(s) is still under study. As a very limited quantity will be required, a fast and reliable solution would be to acquire the FCT signal using a modular oscilloscope card integrated into the ESS EPICS control system. Although this solution will provide a more limited functionality compared to the existing system, it is believed to be sufficient for the purpose.

FPGA SIGNAL PROCESSING

In the previous version of the BCM prototype [1], the ACCT signal processing was done in the control system computer running the Graphical User interface (GUI). This works well for monitoring purposes, but it is not fast and reliable enough to satisfy the MIS requirements. The ESS MIS requires that its entire response time from a fault detection to a beam abort be shorter than 10 µs. Therefore, in the new version, the digital signal processing and the differential interlock logic are implemented in the FPGA. The original firmware of the digitizer card (Struck SIS8300) is upgraded to include the ACCT signal processing.

To synchronize the data acquisition with the repetition rate of the linac, the digitizer card is connected to the ESS timing system. Two 14 Hz triggers from the Micro Research Finland (MRF) timing system are used to mark the start and end of the beam pulse. The triggers are transferred from the MRF timing receiver card to the SIS8300 digitizer either via the front panel or via the backplane connectors. The ESS timing system can also provide a synchronized 88 MHz ADC sampling clock.

As the SIS8300 card has ten analogue inputs, it can be used to sample up to ten ACCTs including up to five ACCT pairs (assuming that no ACCT will be shared between two differential pairs). The ACCT signal is processed in the FPGA to reconstruct the original pulse shape. That includes algorithms for DC level correction, droop compensation, and a moving average filter. After the signal has been processed, a differential interlock comparison is applied. If the difference between the signals in the ACCT pair exceeds a certain threshold, an interlock signal will be sent to the MIS via the front panel interface.

A framework was done to include custom cores in the SIS8300 firmware. The framework includes a custom register array and a custom data-path module. The register array provides an interface to the control system software. The data-path module provides a wrapper for the signal processing modules and the differential interlock module. The signal processing modules are placed in a pipeline one after the other. First, the DC level correction, then the droop compensation, and after it, the moving average filter is applied.

The DC level correction module calculates average of samples before the beam pulse and subtracts this average from samples within the pulse. Thus the negative baseline voltage of the ACCT signal is compensated.

A digital filter with an inverse response of the ACCT sensor and its front-end module is used to compensate for the ACCT droop.

The moving average filter reduces the level of high frequency noise of the ACCT signal.

INTERFACING TO THE MIS

In the current design, a digital output port is foreseen on the RTM for its future connection to the MIS. The Machine Protection System (MPS) group requires that a differential current be measured at 6 locations along the linac [2]. The distance between the two ACCTs ranges from 5 m app. to more than 200 m depending on the location. In the areas where the two ACCT signals cannot be directly fed into the same digitizer, an optical fiber link will be used to communicate the ACCT data from one FPGA card to another. The receiving FPGA will then compare the difference between the two ACCT readings, and in case of exceeding a certain threshold, send a beam abort signal to the MIS to shut the beam off. Apart from the differential measurement, the MPS group requires that the beam be shut off under some other fault conditions including an unexpected pulse or a pulse with wrong width/rate. The FPGA code should therefore include algorithms to detect these errors as well. The other functionality of the FPGA will be to aggregate the interlock outputs of the ACCTs, which will be connected to the same digitizer card. The user can then retrieve the time-stamped ACCT data, and check which ACCT has sent a beam abort request first, if a fault happens. In order to satisfy the MPS timing requirements, the response time of the ACCT sensor and its electronics needs to be around 1-2 µs. Two electrical interfaces are currently under study for the interconnection of the ACCT electronics to the MIS, being the CIBU interface [3] from the LHC and an RS-422 based interface from DESY. These interfaces will be tested and evaluated after prototyping them in-house.

TEST RESULTS

The performance of the BCM system has been tested in laboratory conditions. A MTCA.4 crate from Schroff with CPU and MicroTCA Carrier Hub (MCH) from N.A.T. was used. The Bergoz ACCT signal was fed into a Struck SIS8900 RTM and FPGA processed in a SIS8300

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digitiser. The 88 MHz ADC clock and the 14 Hz triggers were received via the backplane from a MRF timing receiver. The beam was emulated by a 2.86 ms pulsed current passing through the ACCT coil.

In Fig. 2, the red waveform shows the ACCT signal before being FPGA processed. The signal has a DC offset of about -0.6 mA and a droop of approximately 5% of the pulse amplitude. The noise amplitude is approximately 1% of the pulse amplitude. The blue waveform shows the signal after it has been processed in the FPGA. The DC offset and droop has been compensated and the noise amplitude has been decreased to 0.15% approximately.

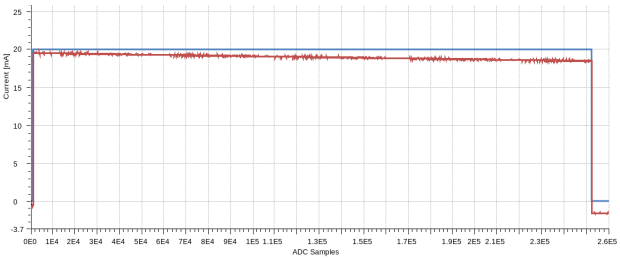


Figure 2: Unprocessed and processed ACCT signal.

Figure 3 shows test results of the interlock response time measurement. The lower two waveforms are the waveform generator pulses emulating the differential ACCT outputs with a difference in their amplitudes. The upper waveform is the digital interlock signal with a response time of 0.8 µs approximately. In the final system, the ACCT-E, the cables and the low-pass filter on the RTM will result in some extra delay, but a response time of < 2 µs is still believed to be achievable.

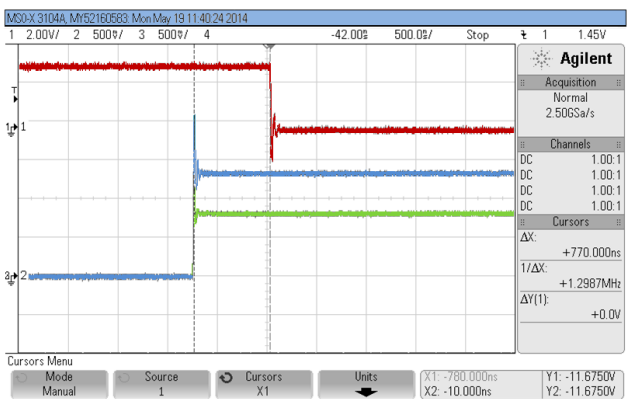
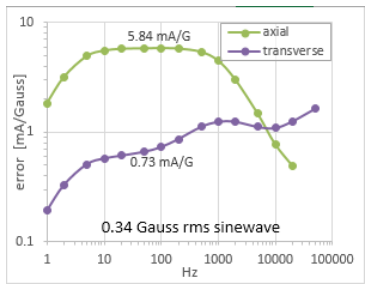


Figure 3: Measured differential interlock output with a response time of 770 ns.

EXTERNAL MAGNETIC FIELDS

The ACCT is a transformer with beam providing a one turn primary through a toroidal core. The droop rate is inversely proportional to the L/R time constant. The high permeability of the core and low impedance of an op-amp configured as a current to voltage converter provides an exceptionally low droop rate. External DC magnetic fields can change the droop rate by affecting the permeability of the transformer core. At about 40 Gauss, the core approaches saturation and the device no longer works. [4]

The effect of external magnetic fields depends on direction. Sensitivity to axial and transverse sinusoidal magnetic fields was recently measured at ESS (Fig. 4).



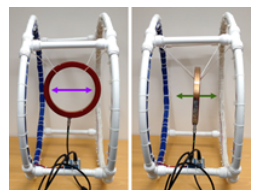


Figure 4: The error from a sinusoidal 1 Gauss external field is 0.7mA for transverse and 5.3mA for axial fields.

SUMMARY AND OUTLOOK

A BCM prototype based on a Bergoz ACCT sensor and MTCA.4 electronics has been set up and successfully tested at ESS. The FPGA of the digitizer card has been programmed to compensate for the ACCT droop, noise and offset thus reconstructing the original shape of the beam pulse with an overall error of < 1%. The ACCT will be interfaced with the future ESS Machine Interlock System to shut the beam off under fault conditions such as a large beam loss, an incorrect pulse width/rate or an unexpected pulse. The system is currently being improved in the following areas: a digitizer card with a larger FPGA for the foreseen signal processing, a digital interface to the Machine Interlock System, differential ACCT signal transmission to the ACCT RTM, an optical link for differential beam current measurement over large distances and an appropriate ACCT shielding against external magnetic fields. It is planned to use a new version of the system in 2015 for the LEBT commissioning.

REFERENCES

[1] H. Hassanzadegan et. al., WEPF30, proc. IBIC2013.
[2] R. Schmidt et. al, "Architecture of the ESS Beam Interlock System", internal report.
[3] B. Todd et. al., "User Interface to the Beam Interlock System", CERN TE department document, July 2011.
[4] H. Bayle et. al., "Effective shielding to measure beam current from an ion source" Rev. Scient. Inst. 85, 02A713 (2014).