DEVELOPMENT OF NEW DATA-TAKING SYSTEM FOR BEAM LOSS MONITORS OF J-PARC MR

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Abstract

A new data-taking system has been developed to improve frequency responses and dynamic ranges of beam loss monitor systems. It consists of newly designed isolation current to voltage converter using analog photocouplers and a VME-based 24 bit ADC system. The conversion factor and the -3dB bandwidth (BW) of the new amp is 1 MV/A and 100 kHz, respectively. The waveform data of 1 MS/s, 1 KS/s, and integrated data are generated and these are compared with alarm levels for the machine protection system (MPS). The system is controlled by the EPICS. In this paper, the system is described.

INTRODUCTION

It is important to minimize the component's activation induced by beam losses for the high power hadron accelerator like Japan Proton Accelerator Research Complex (J-PARC), where the designed output power of the Main Ring synchrotron (MR) is 750 kW. The inevitable beam loss should be limited up to that of 0.5 W/m taking into account the present hands-on maintenances scenario except for the collimator area and the slow extraction area.

The beam loss monitor system reveals beam lost areas, beam loss timings, and beam loss power generally, however the difference of the DCCT output gives the precise beam loss power and the activation survey during a beam stop for maintenances reveals beam loss points.

A 1.1 atm Ar+1 % CO_2 gas proportional counter (P-BLM) is adopted for the main detector for the beam loss monitor system of 3 GeV RCS to 50 GeV MR beam transport (350BT) and MR. As for the MR, the 216 P-BLMs are mounted on each Q-magnet 360 mm apart from the side of the Q-magnet (848 mm from beam line). The additional P-BLMs are used at some special areas like injection line including collimator area, RF system, slow extraction area, fast extraction area, and beam dump line. The P-BLMs are used as an alarm system for an extraordinary beam loss increment due to unforeseen troubles of the machine components, rare beam instabilities, and miss operations. The output waveform from the front-end amplifier and its integral per beam cycle are compared with each reference voltage using analog comparators, and then output alarms to the Machine Protection System (MPS) within 10 μs to deliver a beam to the beam dump within 100 μs. The overall P-BLM system is described in elsewhere [1].

An air filled ion-chamber using coaxial cable [2], Air Ionizing Chamber (AIC), are also used. The long type AICs (long AIC) are mounted on cable racks which is 3m apart from the beam line. However the data-taking system for this detector is not yet on line.

The present BLM system needs to be upgrade to make countermeasures against the gain degrade problem of the P-BLM and to meet requirements the coming high power operation to 750 kW. The present issues of the system are described in the next chapter. The upgrade plans are described in ref. [3]. In this paper, we described the newly developed front end isolation amplifier, and ADC system.

ISSUES OF THE PRESENT BLM SYSTEM

With the high gas gain property of the P-BLMs, ×20000 at the maximum, the low level beam loss had been investigated in good resolution at the early stage of the MR tunings. However, the following issues have become severe with increasing the beam power.

In generally, gas gain of the proportional counter depends on the output current intensity because the positive ion sheath around the anode effectively degrades the bias voltage [4]. Thus, the intense output current induced by the high level beam loss makes bare gas gain decrease, and the system underestimates the beam loss intensity. Hendrics formulized analytically the gas gain in DC and its equation shows that our P-BLM anode current should be limited up to 1 μA in DC which result in the gain decrease by 10 % at the maximum. Satou et al [5] shows semiempirical formula of gas gain depending on the output charge per beam pulse for P-BLMs at 350BT.

The present front-end amplifier has inadequate current to voltage conversion factor of 100 kV/A and the band width of the system is DC to several hundred Hz depending on the input capacitance of long cable of 100 to 300 m. A new front-end amplifier with high conversion factor of 1 MV/A and high speed of 100 kHz is needed. To improve the dynamic range of the system, the 24 bit ADC has been developing.

NEW FRONT-END AMPLIFIER

To improve the gain and frequency response, the simple choice is to adopt trans-impedance circuit, the current-to-voltage (I-V) converter (see Fig. 2) using low noise op-amp with large Gain Bandwidth Product (GBP). The expected -3dB bandwidth of the system is $BW = (GBP/2\pi R_f C_i)^{1/2} = 18$ kHz for $R_f = 1$ MΩ, $C_{in} = 30$ nF, GBP = 60 MHz, where R_f is feed-back resister and C_{in} is input capacitance. The R_f is the current to voltage conversion factor. To obtain the 100 kHz amp, the op-amp with GBP > 1.9 GHz are needed. However a number of a high speed op-amp with low noise and low temperature drift is restricted.

To improve BW, naive choice is to reduce R_f to 100 kΩ for example, and use the 20 dB gain amp additionally after I-V converter. It improves the BW directly proportional to $(R_f)^{-1/2}$. But the later gain amp increases the thermal noise density. It is expressed as $(4K_BTR_f)^{1/2}$, where K_B is Boltzman's constant and T is temperature in Kelvin, thus the noise is then increases by the factor $10 \times (100\ \mathrm{k\Omega})^{1/2}/(1\ \mathrm{M\Omega})^{1/2} = 3.2$.

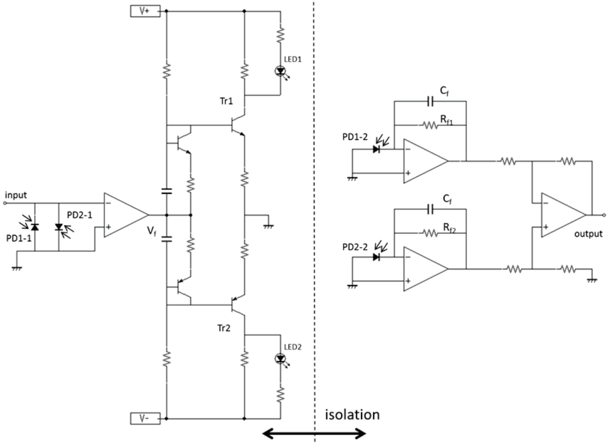

Figure 1: Basic circuit of the new I-V converter.

The new I-V converter (new amp) was developed to improve the BW. The Figure 1 shows the basic circuit of the newly developed isolation amplifier using photocuplers, HCNR201 from Avago [6]. The photodetectors PD_{1-1} (PD_{2-1}) and PD_{1-2} (PD_{2-2}) are coupled with LED1 (LED2), where transmission coefficients of the current between PD_{1-1} (PD_{2-1}) and PD_{1-2} (PD_{2-2}), $\alpha = I_{PD1-1}/I_{PD1-2}$ (I_{PD2-1}/I_{PD2-2}), is 1.00 ± 0.05. Its operation frequency is DC to 1 MHz in typically.

When the signal current I_{in} flows to the non-inverting input terminal of the op-amp, the output terminal voltage V_f and the two transistors Tr_1 and Tr_2 control the LED bias voltage so as to shunt the input current through PD_{1-1} and PD_{2-1} as I_{PD1-1}-I_{PD2-1}=I_{in}. The output currents from the PD_{2-1} and PD_{2-2} are converted using normal I-V converters and following differencial amplifier make I_{PD2-1} -I_{PD2-2}. The thermal noise is then $(2)^{1/2}(4K_BTR_f)^{1/2}$. The feedback network is tuned as $PD_{1-1} = PD_{1-2} = 0.1$ μA as the AB class amplifier.

Figure 2 shows the frequency response and the noise density of the I-V converter and the new amp with the feedback resisters $R_f = R_{f1} = R_{f2} = 1$ MΩ, where the input capacitance set as $C_{in} = 47$ nF and the low noise op-amp AD8065 (GBP = 60 MHz) was used. The gain peeking can be compensated by putting the feedback capacitance parallel to the feedback resister as $C_f = 10$ pF. The BW of the new amp is limited by the stray capacitance parallel to the feedback resister. As can be seen in the figure, new amp's BW is about 4 times higher than that of the I-V converter.

A calculation of the noise density of the I-V converter e_{no} is also shown, where thermal noise of the feedback resister e_R, shot noise of the input bias current i_i, and input voltage noise e_i are taking into account. The calculation shows good agreement with the data lower than 20 Hz. At higher frequencies additional noise may come from another voltage source e_n schematically shown in the figure. The voltage noise e_n is converted to the current noise through the C_{in}, and the noise current converted to noise voltage with the closed loop gain. The new amp's noise density is quite similar to that of the I-V converter. The detail of the noise density for the new amp is now under investigation.

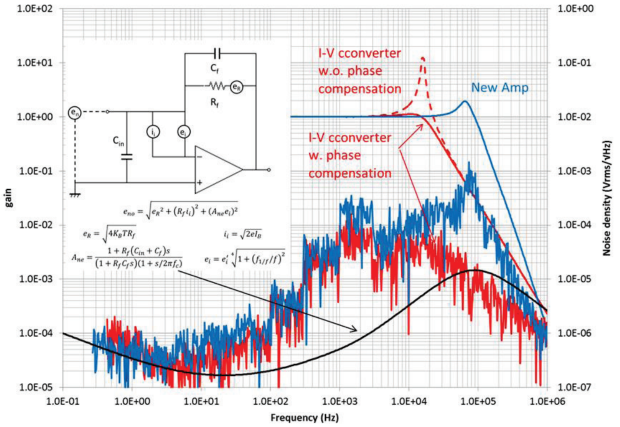

Figure 2: Frequency response and noise density of the normal and new designed I-V converter.

Some parameters of the new amp were also measured. The Total Harmonic Distortion (THD) is 90 dB at 1 kHz, and the Isolation Mode Rejection Rate (IMRR) is 94 dB at 50 Hz and it rolls off as -20 dB/dec. The offset drift is important for this system. To minimize it, delicate tuning of the two conversion resisters R_{f1} and R_{f2} are needed to compensate the difference of the transmission coefficient α. After tunings, the offset drift was thus 5 μV/K. This results in an input equivalent offset drift of 10 pC/K for 2 s charge integrations.

ADC SYSTEM

The VME based ADC system has been developed [7]. The Figure 3 shows the block diagram of the system. One unit system includes 6 ADC boards (4 input/board), 1 timing board, and 1 commercial CPU board. An input signal is processed by the 24 bit ADC, and offset subtraction, digital filtering, waveform integration, and signal level monitoring are made in the FPGA in an ADC board. The front end amplifier of the ADC has BW of DC-300 kHz, noise level of 100 uVpp, and THD of 80 dB. The Figure 4 shows the data processing in the FPGA schematically.

To estimate the offset level, the waveform data are integrated for several 20 ms, between trigger 1 and trigger 2, to avoid 50 Hz electricity noise prior to the beam injection while the switch in front of the isolation amp open to cut current from the BLM detector. The offset subtraction is made after trigger 2. This process is made at each MR cycle.

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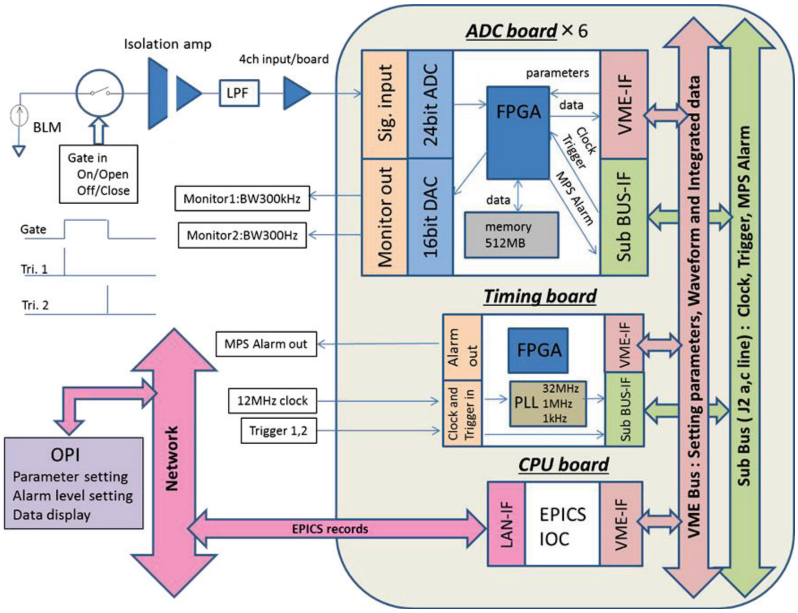

Figure 3: Block diagram of the BLM data-taking system.

Although at this moment, there are no beams in the 350BT and MR, the residual dose induced current is superimposed. The offset level between trigger 2 and beam injection shows the current. The current should be extracted from the following beam loss signals. Using the good offset stability of the ADC and high gas gain of the P-BLM, a long-term on-line monitoring of the residual dose during beam stops will also be realized.

After offset subtraction scheme, at first, the 1 MS/s data are generated and compared with the MPS reference level in real time, the alarm level 1 as in the Figure 4. The data are subsequently input to a digital integrator. There the integrated waveform is compared with the alarm level 2. Once these waveforms exceed each alarm level, the system outputs alarms through VME sub-bus to the timing board which have output terminals to MPS.

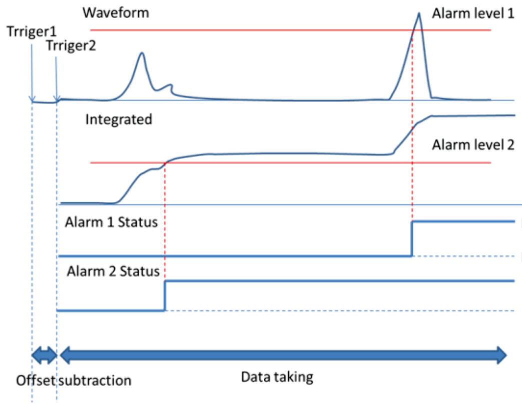

Figure 4: Schematic drawing of the signal processing at the FPGA.

The 1 MS/s data are downsized to 1 KS/s data. The waveform data of 1 MS/s, 1 KS/s and integrated value are stored in the 512 MB DDR3 memory. The memory can store the past 18 s length data and data is updated at each MR cycle. The data are input to 16 bit DAC and output to the monitor out terminal so as to monitor waveforms using an oscilloscope. The data takings, parameter settings, and MPS alarm level setting are all made by using EPICS records.

CONCLUSION

We have developed the new I-V converter using photocouplers to improve the BW from several hundred to 100 kHz and conversion factor from 100 kV/A to 1 MV/A. The new amp shows BW of about 4 times higher than the normal I-V converter without remarkable noise density degradation. However more investigations are needed to understand the noise density profile.

The 24 bit ADC system with the noise level of 100 uVpp and THD of 80 dB was developed. To improve offset level stability, the shot by shot offset subtraction scheme was adopted. It is expected that, by comparing the offset level, residual dose induced current which is superimposed on the real beam loss signal can be monitored. By using the high gas gain of the P-BLM the on-line monitoring of the residual dose during beam stops can be made.

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