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BEAM TRIP ANALYSIS BY BUNCH-BY-BUNCH BPM SYSTEM IN BEPCII*

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Abstract

A new bunch-by-bunch beam position measurement (BPM) prototype has been designed and built to monitor the beam instability and analyse the beam trip in the BEPCⅡ (Beijing Electron-Positron ColliderⅡ) machine. The broadband electronics system which employs fast analogy digital converter (ADC) and field programmable gate array (FPGA) can obtain the beam information bunch-by-bunch with high bunch-to-bunch isolation. Therefore, the system can analyse the beam motion bunch-by-bunch both in time domain and in frequency domain. In this paper we will present the system architecture and discuss some beam trip analysis result, such as RF trip, beam instabilities and magnet power instabilities.

INTRODUCTION

The performance of storage ring accelerator can be greatly degraded due to beam trip as the result of various subsystem failure. For the collider, the beam trip can significantly reduce the integer luminance. Analysing the causes of beam trip by post-mortem diagnose system can help us to improve the reliability of subsystem and reduce troubleshooting effort [1]-[3].

Bunch-by-bunch measurement is widely used in feedback system for control of coupled-bunch instabilities in circular accelerators. In practice, bunch-by-bunch data can be used to analyse the beam instabilities and beam trip events [4]. A bunch-by-bunch BPM system has been developed to measurement beam position bunch-by-bunch, and it is effectually to analyse the beam trip events.

BEPCII is an electron-positron double-ring collider which is designed to operate at about 1A beam current. Some major deigned parameters related to the beam trip analysis are listed in table1.

Table 1: Main Parameters of BEPCII

Parameters	Electron ring	Positron ring
Circumference	237.53m	237.53
RF frequency	499.8MHz	499.8
Harmonic number	396	396
The number of RF cavity	1	1
Revolution frequency	1.2621MHz	1.2621MHz
Minimum injection bunch interval	4ns	4ns

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BUNCH-BY-BUNCH SYSTEM

Typically, the system consists of the front-end, the digital signal processor board which contain ADCs and FPGA and the upper control computer.

The important point has to be made before we delve into the details of the front end. Based on the Nyquist-Shannon sampling theorem, it's expect that the input signal to be band-limited within the half of sampling rate to prevent aliasing. The bunch-by-bunch measurement system operates at a sampling rate of RF frequency, and the aliasing is used to achieve high isolation between neighbouring samples. The system analogue bandwidth is larger than the first Nyquist band and all elements of the front end should have large analogue bandwidth to prevent the bunch to bunch coupling [5].

Front-end and ADC Sampling

The schematic of the front-end is sketched in fig.1. The four channel analogue signals are normally generated by pickup with 50Ohm termination. The attenuators adjust the amplitude of the analogue signal. As the four cables are not in the same length, the phase shifters adjust the signal phase in accordance with each other.

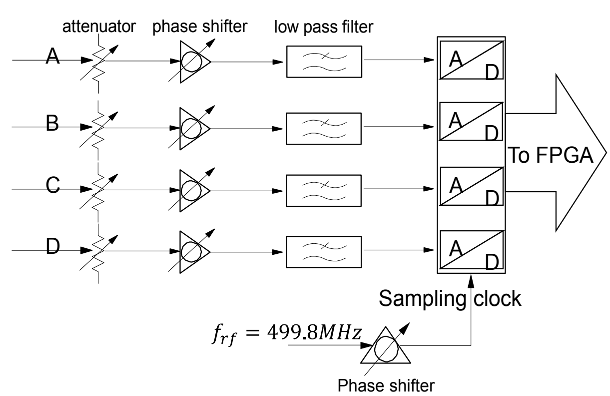

Figure 1: Layout of front-end.

The digital signal processor board has four 14 bits resolution ADCs which work at the sampling rate of 499.8MHz. As the ADC analogue bandwidth is form DC to 800MHz, it means that the pulse width of analogue signal is broaden by pass the 800MHz low pass filter, and it can't achieve completely isolation between neighbouring samples with 499.8MHz sampling rate. However, for BEPCII injection pattern, the minimum bunch interval in is 4 ns, and it can achieve high isolation for each bunch.

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The sampling clock signal is comes from the accelerator main timing clock which has high stability, and it is also adjusted by a phase shifter to make that all the ADCs sample at the top of the pulses.

Digital Signal Process and Store

The hardware system can realize to store the four channels ADC data at the rate of 499.8MHz. The FPGA control logic transfers the bunch-by-bunch data from the ADC model to a 4GByte DDR3 memory. The DDR3 memory gives us ability to store over 2 second continuous bunch-by-bunch data, and it is enough for us to analyse all beam trip events. A schematic view of the data acquisition and control logic is given in Fig.2.

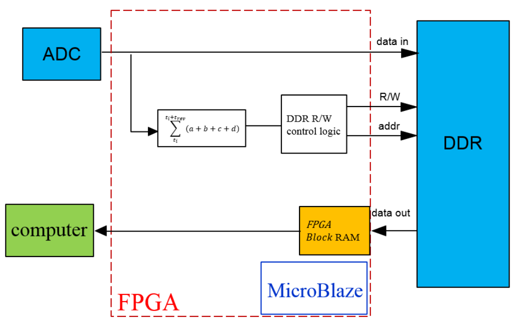

Figure 2: The diagram of digital signal process.

The data form ADC model is also used to calculate the current in the storage. Base on the sampling principle in system, regardless of the affection of oscillation, the current in the storage ring can be gave by:

$$I_{all} = k\sum_{i=1}^{h}(a_i + b_i + c_i + d_i)$$

Where h is the Harmonic number, k is the calibration coefficient.

The DDR read/write control logic writes the data to DDR until there are almost no current in the storage. In other words, the DDR3 write stop signal is generate by the data from formula above, and the system doesn't need any trigger signal input. After the system has detected the beam trip event, control logic transports the data from DDR through FPGA block RAM to upper computer.

DATA ANALUSIS AND EXPERIMENTAL COMPARISONTION

The BEPCII storage rings have been operated at high beam current, therefore, there are many beam trip events. To study the beam trip in the BEPCII, more than 200 beam trip events have been collected. By analysing the bunch-by-bunch system data which from unexpected beam trip events and some well-designed experiments, some mechanisms of beam trip is clear.

RF Trip

Almost all of the beam trip events in BEPCII storage rings are accompany with RF trip. Actually, the beam trip process which case by RF trip is very fast (~200us), and it is very difficult to analyse by general post-mort diagnosis system. By the bunch-by-bunch system, we can easily distinguish RF trip events.

The relative bunches current which can be obtain from the sum of four button signals, and the bunch current is uniform in the process of beam trip. There is no abnormal oscillation in all bunches. The sum signal of bunch 1 in the position storage ring is shown in Fig.3. Combining with the waveform of the dipolar signal from the positron storage ring BPM, it is clear that the beam signal was shifted relative to system sampling clock. The sampling clock is comes from the stably source of accelerator timing clock directly, so the bunch longitudinal phase has changed violently. The bunch longitudinal phase change means that the beam energy has changed. In conclusion, this phenomenon is obviously caused by RF trip.

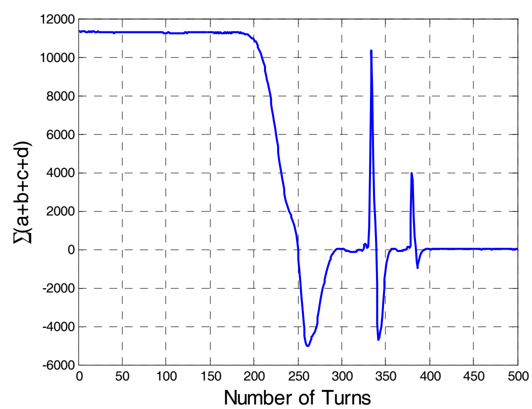

Figure 3: Bunch sum signal case by RF trip.

The Fig.4 shows that the electron storage ring RF (RFE) and positron storage ring RF (RFP) are trip almost at the same time. The data also indicate that all the beam trip in two storage rings is cause by RF trip, and RFE trip earlier than RFP trip about 0.3ms. There is no obvious oscillation in both rings before RF trip, and the electron beam trip has no affection the positron beam motion.

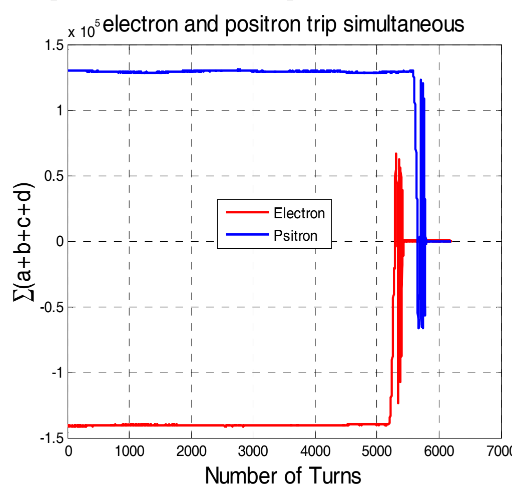

Figure 4: Double RF trip simultaneously.

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Power Instabilities: Beam Resonance

As we known the resonance theory in storage ring accelerator, the resonance strength generally get weaker with increasing order, and a particle beam would not survive on an integer or a half integer resonance all other resonances are basically survivable [6].

Take the analysis of an typical resonance beam trip event. The unequal current loss in each bunch shown in Fig.5, and the bunches in the tail of bunch train loss faster may cause by the affection of wake field. Though the spectrum analysis of each bunch, the resonace at half integer can be found in frquency spectrum.

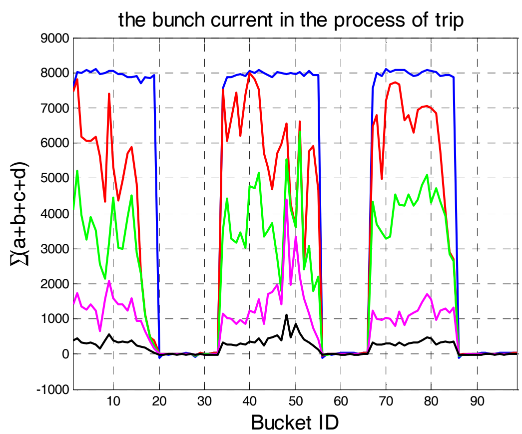

Figure 5: Sum signal in the process of trip.

Actually, this beam trip events is cused by the instability of the power system. Based on the large data store in system, the analysis of whole beam loss process with about 1 second can be done. The whole process ananlysis is shown Fig.6, the the horizontal tune shifted to half integer, and the beam resonance results in part of beam loss, and then lead to the RF trip.

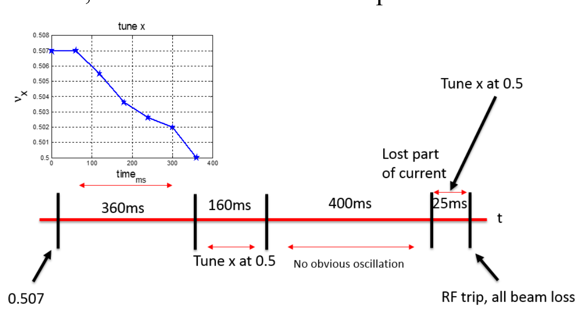

Figure 6: whole process analysis.

Beam Instabilities

The beam feedback system is widely used in circular accelerators for control of coupled-bunch instabilities. But in BEPCII storage ring, the feedback system does not always works well to restrain the coupled-bunch instabilities under high beam current, and there are some beam trip events caused by coupled-bunch instabilities.

The analysis result of a typical beam trip cause by beam instabilities is shown in Fig.7. The bunch current in the process of beam trip is indicate that some bunches at the tail of second train was lost. The bunch position root-mean-square (RMS) value is indicate the oscillation amplitude. The bunch position RMS is calculated based on 30000 turns in horizontal and vertical direction before the beam trip. The figure of beam oscillation amplitude indicates that the instabilities is increase along the bunch trains, and it obvious that the tail bunches will firstly loss. Besides, the frequency-domain analysis of the bunch data can get that the tune in horizontal and vertical direction are all normal. Finally, the RF was tripped as the result of beam instabilities.

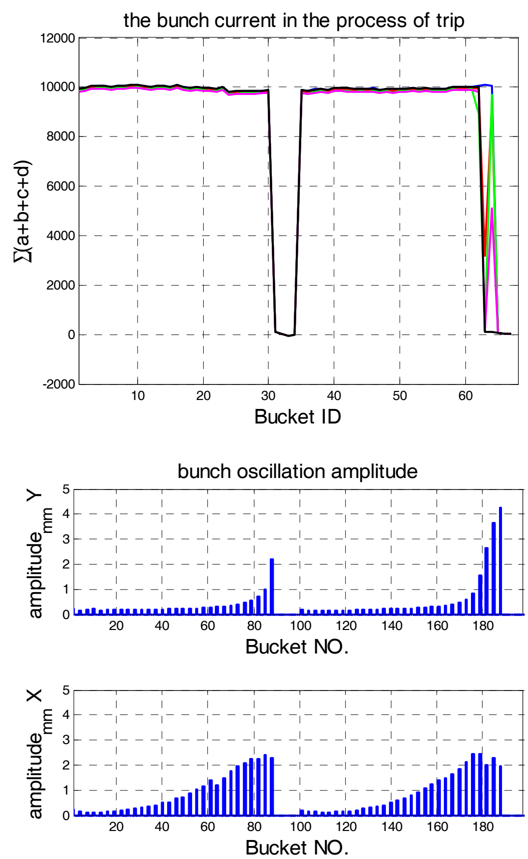

Figure 7: Beam trip cause by instability.

CONCLUSION

The Trip even analysis can aids of learning appropriate action to improve sub-system, to avoid dangerous operation condition, as consequently improve the whole accelerator system stability. To study the beam trip is very urgent for the BEPCII to get higher luminance. It is proved that the bunch-by-bunch system shows the excellence at the aspect of beam trip event analysis. We had established a bunch-by-bunch BPM system for BEPCII storage rings, and many mechanisms of beam trip had been cleared which are summarized in this report.

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