AN FPGA BASED CONTROLLER FOR THE MICE TARGET*

C. N. Booth, P. Hodgson, E. Overton, M. Robinson, P. J. Smith, The University of Sheffield.
J. Leaver, K. Long, Imperial College, London.

Abstract

The MICE experiment [1], uses a beam of low energy muons to test the feasibility of ionization cooling. This beam is derived parasitically from the ISIS accelerator at the Rutherford Appleton Laboratory. A target mechanism has been developed that rapidly inserts a small titanium target into the circulating proton beam immediately prior to extraction without unduly disturbing the primary ISIS beam. The original control electronics for the MICE target was based upon an 8-bit PIC. Although this system was fully functional it did not provide the necessary IO to permit full integration of the target electronics onto the MICE EPICS system. A three phase program was established to migrate both the target control and DAQ electronics from the original prototype onto a fully integrated FPGA system that is capable of interfacing with EPICS through a local PC. This paper discusses this upgrade program, the motivation behind it and the performance of the upgraded target controller.

THE MICE EXPERIMENT

The goal of the international Muon Ionisation Cooling Experiment is to construct a section of cooling channel long enough to demonstrate a measurable cooling effect, i.e. the reduction in transverse emittance of a muon beam by the order of 10%.

A range of particle detectors will be used to measure the cooling effect particle by particle with high precision, in order to achieve an absolute accuracy on the measurement of emittance of 0.1% or better. The emittance measurements will be performed with muon beams of various momenta within the range of 140 to 240 MeV/*c* and a variety of beam optics and absorber materials will be employed. The primary beam-line for the experiment has been constructed and commissioned and work is now focussing on installing the major components of the cooling channel.

MUON SOURCE

The ISIS accelerator, at which MICE is housed, is located at the Rutherford Appleton Laboratory in the UK. It accelerates protons from a kinetic energy of 70 MeV at injection to 800 MeV at extraction, over a period of 10 ms. The next injection follows 10 ms later.

The MICE target has been designed to operate parasitically on the ISIS synchrotron, inserting a narrow titanium shaft into the proton beam during the last 2 ms prior to beam extraction. Pions created by the interaction are collected, with their subsequent decay providing the source of muons for the MICE experiment.

During the 10 ms acceleration period, the beam at the target location shrinks from a radius of ~48 mm to ~37 mm. Since the exact position of the edge of the beam and the intensity of the halo show some variation, the insertion depth of the target is adjustable. The MICE target must be completely outside the beam during injection and acceleration, being driven to overtake and enter the beam in the 1-2 milliseconds before extraction when the protons are close to their maximum energy. The target must then be outside the beam envelope again before the next injection. To achieve this, the acceleration required of the target is of the order of 700 - 800 ms^{-2}.

MICE will only sample the beam up to a rate of a few Hz, so target actuation is on demand, synchronised to trigger on signals from both MICE and ISIS.

Two targets have operated on ISIS since the experiment started. The first target drive was installed in ISIS during 2008 and operated successfully for over 100,000 pulses. A second upgraded design was installed in 2009 and operated for over 550,000 actuations until July 2011. A new target will be installed on ISIS later this year.

TARGET CONTROLLER

The target control system is composed of several functional units that interconnect as a complete system. Loosely this system comprises of the target positional measurement, the target power supply, the control electronics and the data acquisition (DAQ). A complete description of the target mechanism itself can be found in the accompanying target paper at this conference [2], and so will not be covered here.

The position of the target shaft is measured with an optical quadrature system. The top of the target shaft carries a readout vane in the form of a comb with a pitch of 0.6 mm. The teeth on the comb interrupt two laser beams, and the modulation of these beams is used to determine the change in the target's position to a resolution of 150 µm. A third beam fixes the absolute position. As the target assembly operates in a high radiation environment, all active optical and electronic components are situated remotely, and signals are delivered to and from the readout via optical fibres.

There are a number of modes of operation of the target drive. These include the reversible movement from a powered off state also known as 'park' to a raised 'hold' position, 'enabled', when the electronics is waiting for a trigger and 'actuating', the triggered rapid insertion into the beam. All require the appropriately phased application of currents through the stator coils. (These coils are wired

*We wish to thank the MICE collaboration and the ISIS Division at the STFC Rutherford Appleton Laboratory for the invaluable help and support in the performance of this work. We also gratefully acknowledge financial support from the STFC.

in a three-phase star configuration.) The three-phase, bi-directional supply to the coils is switched through six pulse width modulated (PWM) Integrated Gate Bipolar Transistors (IGBTs) powered by a pair of capacitor banks.

The capacitor banks are charged using a pair of 4 A capacitor charging units. During actuation an initial current of ~60 A is switched through the stator coils, although this current does droop by about 15% during the actuation cycle. The two capacitor banks are wired in series with the mid-point grounded. This ensures an even switching voltage across the phases, typically +/- 115V, minimising voltage stress on the coils.

The original design for the target controller is based around an 8-bit 16F871 PIC microcontroller. This orchestrates the sequencing of the switching of the three phase supply and manages the PWM so that the target can be moved from unpowered to hold (levitating) to actuating and back again. The controller was built on Veroboard which limited the design to the use of dual in line (DIL) ICs. System control was all local to the electronics thereby lacking the ease of use that a remote GUI can provide.

Feedback from the PIC based system is inadequate; both the status and performance of the target system have to be inferred indirectly from the DAQ readout. This means that the system is unintuitive and consequently it can only be operated by an expert. Additionally the lack of integration with the MICE controls means that operational parameters can only entered into the MICE controls database manually; this is tedious and error prone.

The DAQ for the target control system is based upon a National Instruments PCI 6254 card but due to software driver issues under Linux only the analogue inputs on this card are currently utilised. The target DAQ monitors the target position, ISIS beam intensity and ISIS beamloss as a function of time.

Because this system was originally intended to be just a test bench in the laboratory it was clear from the outset that this controller could not be permanently used to operate the MICE target on ISIS. An FPGA was considered to be the ideal platform on which to base improved control electronics as it permits many processes to be run in parallel, permitting integration of the circuitry onto a single synchronous chip. This upgrade was to take place over three phases, the first two phases focusing on the control with the third phase focusing on the DAQ. Details of these phases will be described shortly.

THE FPGA BOARD

The FPGA board used for the target control upgrade is based upon a Xilinx Spartan-3 XC3S1000-5FG676 FPGA and a Cypress CY7C68001 USB controller. This board, named the USBDAQ, had been already been designed at Imperial College as a flexible general purpose FPGA IO board for use in HEP experiments. The board has both 40 MHz and 100 MHz external crystal clocks, although with the FPGA's onboard digital clock manager, a range of clock frequencies is possible. The majority of the FPGA's IO pins are accessible to the user via several DIL headers placed around the board's edges. This board has been used on previous experiments and it is well tested and debugged. A photo of a completed USBDAQ board is shown in figure 1.

The Cypress USB chip permits USB data exchange via individual registers or by block transfer of data. The VHDL processes that permit the FPGA to communicate with the USB controller on the USBDAQ board had already been written and can be interfaced to using VHDL both easily and flexibly. Therefore this section of the design could be treated as a black box and utilised as required, easing the transition of the target control design onto an FPGA.

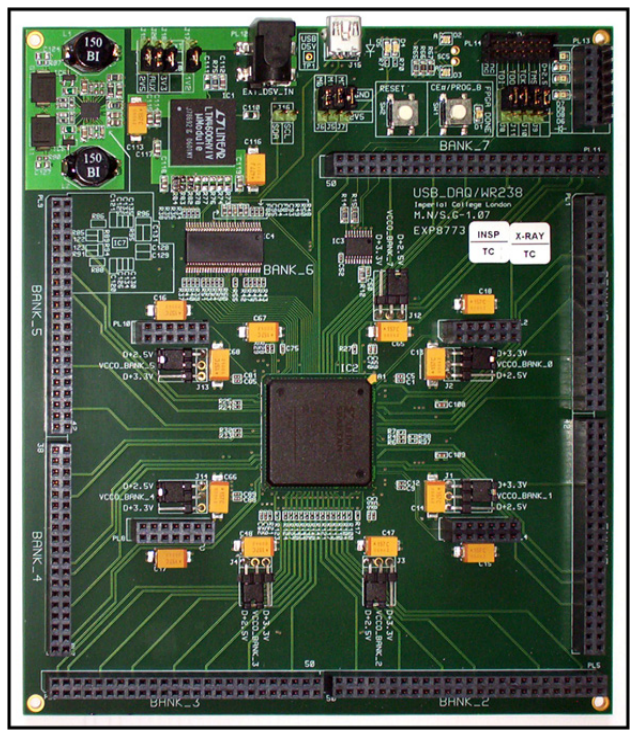

Figure 1: The USBDAQ board forms the heart of the new target controller. It utilises a Spartan-3 XC3S1000-5FG676 FPGA (centre) and a Cypress CY7C68001 USB controller (the SOIC on the upper left). The board was designed to maximise the accessibility of the FPGA's IO as can be seen from the extensive array of DIL headers.

PHASE ONE UPGRADE

The purpose of the phase one upgrade was to move the control algorithms onto the FPGA, establish computer control of the target mechanism via a GUI and to improve the monitoring of the controller via suitable feedback over the USB interface. With the exception of the USB socket on the FPGA board and the external controls, most of the IO interfacing to the controller was to remain the same. Therefore a hybrid system was produced with the FPGA at the heart of a system surrounded by Veroboard based

IO cards that connected to the FPGA via a purpose built 5V/3.3V level translator PCB.

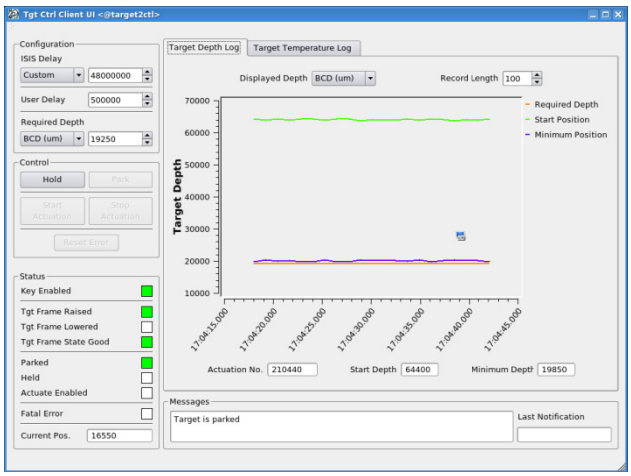

Figure 2: The target controller client GUI presents a turn-key solution to MICE target operations.

Internally target control is managed via a hierarchy of finite state machines. Twenty six 32-bit USB registers are used to both set and read back operational parameters from the target controller. The status registers are logged continuously by the server PC giving an actuation by actuation account of the status of the target controller. Most of the target setup parameters are stored in an XML file which makes it much easier to fine tune various control parameters.

Error states are managed in a hierarchal fashion and wherever possible the system is designed to stop operation of the target in a controlled manner when an error state occurs.

A GUI based target control client was written; this communicates with a server process via EPICS. The server process then connects directly to the USBDAQ board over the USB interface. The EPICS Process Variables are monitored by the MICE Controls and Monitoring system providing an automatic record of target settings for every MICE run. Additionally the server/client setup allows the client to be run remotely which has proven to be very useful with the MICE target test system.

Originally it was planned that the new phase one target controller was to be tested for a short period on a second test target system before being installed on the main system on the ISIS beamline. However the controller proved to be so useful on the test system, providing much needed additional diagnostics when testing various bearing designs that the decision was made to leave it in situ until the phase two controller was ready.

PHASE TWO UPGRADE

The phase two upgrade completes the target controller upgrade by putting the entire controller's IO onto two purpose made daughter cards that bridge directly to the FPGA board via DIL headers. The higher component density available by using PCBs and surface mount components has permitted several new features to be added, including more digital IO, and digital monitoring and control of the analogue amplifiers used in the position measuring system. The serial peripheral interface (SPI) bus protocol is used to communicate between peripheral integrated circuits and the FPGA on non critical timing signals. The firmware was updated to take advantage of the new hardware and additional internal controls were added to improve the performance of the controller.

At the request of ISIS, phase two also added a Beam Protection System (BPS) signal to the target control system. Several key points in the trajectory of each target actuation are compared to a set of limits. If any of these limits are exceeded, indicating that the actuation was not normal, then the target BPS signal drops; this inhibits ISIS injection thereby preventing the possibility of continuing to put beam onto the target. The limits are determined in software and downloaded to the FPGA over the USB link. Changes in the target's operational parameters from the GUI automatically change the BPS limits.

PHASE THREE UPGRADE

The original plan for the phase three upgrade was to build a stand-alone FPGA based DAQ for the target system. However a software upgrade has been identified that should permit the current National Instruments card to be used to its full capacity. Successful implementation should provide the required DAQ functionality and would be a more cost-effective solution than a full redesign of the target controller DAQ.

CONCLUSION

The phase two controller was recently commissioned in building R78 at RAL before it was moved to the MICE local control room in readiness to run the ISIS target in autumn. This is a significant upgrade to the PIC-based controller and will finally allow the MICE target to come under the control of the MICE EPICS system. The flexibility of the FPGA system means that the controller can be easily upgraded or enhanced as required.

REFERENCES

[1] MICE, an international Muon Ionisation Cooling Experiment: proposal to the Rutherford Appleton Laboratory, submitted to CCLRC and PPARC on the 10th January 2003. http://mice.iit.edu/micenotes/public/pdf/MICE0021/MICE0021.pdf

[2] C. Booth *et al.* Design and Performance of The MICE Target. Contribution to the International Particle Accelerator Conference, IPAC'11, 4th – 9th September 2011, San Sebastian, Spain. ID 3224. (Proceedings in press.)