NEW TECHNIQUES IN THE SYNCHRONIZATION OF HIGH-FREQUENCY MULTICHANNEL ACQUISITION SYSTEMS

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Abstract

Today, high-speed digitizer systems operating at well above 100 MSa/s are being used in a diverse range of applications including operation of single-pulse linear induction accelerators for flash radiographic facilities, neutron energy measurement through time-of-flight, and propulsion research. A growing number of such applications require simultaneous measurement of high-frequency signals over many channels.

Most of today's high-speed digitizers or oscilloscopes feature a maximum of only four channels. For applications requiring more than four channels, and needing very precise time correlation between channels or accurate phase of continuous signals, it is necessary to synchronize the sampling clocks for the multiple instruments within the system.

INTRODUCTION

High speed digitizers integrate analog signal conditioning, analog-to-digital converters (ADC), acquisition memory, along with the necessary clock, reference, triggering, power supplies, and bus interconnects, to create modules capable of accurately capturing and digitizing a high-speed analog signal, and passing the acquired digital amplitude and time data to some host processor. They are the data acquisition components of choice for large multichannel systems. This is due, in part, to the ability of these modules to provide fast data transfer of the acquired data, to combine the latest in high-resolution, high-speed ADC components, along with the high level of integration that provides this performance in a small, low power package.

Figure 1 shows a very simplified block diagram of a digitizer module. The signal to be captured passes through front-end signal conditioning (FEA) to optimise gain and offset for the subsequent ADC component. The acquired digital data is then stored to memory, transferred for real-time processing in an FPGA, passed to the host processor, or any combination of these functions.

Digitizers are available in various standards, including PCI, PXI, VXI, NIM, and more recently based around the high-speed PCI Express® bus, with PCIe®, PXIe and AXIe modules now available. Use of standard busses and formats allows easy system interconnection, and the creation of multichannel systems through the addition, or replacement of modules.

Multimodule Synchronisation

One flexibility in the use of modular high-speed digitizers is the scalability of the systems created. Digitizers exist with as little as one channel per module, but multichannel modules exist, and systems can quickly be built by stacking multichannel modules within an appropriate chassis or even within a desktop PC.

The requirement to acquire many channels of data is often linked to the requirement of capturing an event, or series of events with an array of multiple transducers. Such applications include coincidence measurements with multiple photomultiplier tube (PMT) detectors, for the detection and measurement of neutron related processes [1], or the detection of low-energy solar neutrinos.

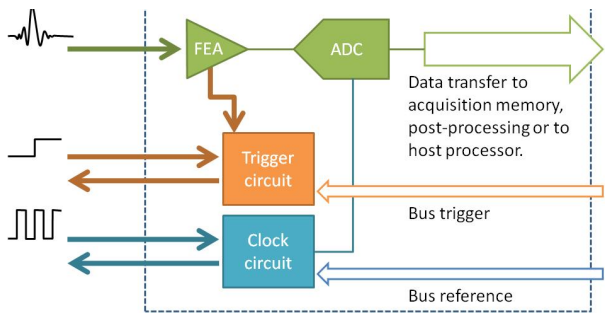

Figure 1: Very simplified schematic of a single channel digitizer module, with trigger, clock and data paths.

These systems often require time synchronised channels, so that temporal correlation can be made between data points.

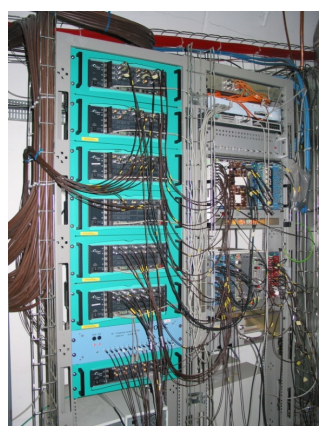

Figure 2: Example of a multichannel digitizer system based around the CompactPCI modular standard. (nTOF experiment: Photo courtesy of CERN, Geneva)

SYNCHRONISATION SCHEMES

Various hardware schemes exist that can be used to distribute clocking and trigger signals for system synchronisation. For the purposes of this discussion we

will take the example of a 50 channel system running at 2 GSamples per second.

External Synchronisation

For highly demanding applications, synchronous sampling across multiple instruments can be achieved using a common 10 MHz clock reference provided by an external high-stability source.

As already expressed, it is relatively difficult to split and propagate an external 2 GHz ADC clock to multiple units without degrading the clock signal through added distortion and jitter.

Alternatively it's possible to use the local reference clock generated by one digitizer to provide the 10 MHz reference to fix the clock phase between master and slave modules, as shown in Figure 3. This removes the requirement for an additional clock source, but leaves one important challenge: measuring sub-nanosecond time delays between the synchronous samples of different channels.

When the sampling-clock skew between channels must be precisely measured, we have previously shown that a sine-fit method will allow effective suppression of most error sources to within 1 picosecond [2].

With typically between 2 and 8 channels per digitizer unit, a 50 channel, 2 GSa/s system could require fanning out the reference to between 6 and 24 individual modules. This presents its own technical issues. Using this scheme requires the preparation of the individual machine states of the digitizers through software, and any changes in state would have to be communicated through the host processor.

Proprietary Clocking Schemes

With Agilent Acqiris digitizers, synchronous sampling can be achieved across several modules with the proprietary AS Bus system. This distributes trigger and clock signals across adjacent digitizers through a front panel dongle. This synchronisation scheme is made possible through the use of a combined clock and trigger ASIC, that was designed specifically for this purpose. Though technically difficult, as the distance between adjacent modules is of the order of centimetres, and known to within a recognized tolerance, it is possible to propagate the sampling clock, of up to 2 GHz, using an external hardware component. With this scheme not only are the clock and trigger delays propagated, there is also a synchronisation of machine state enabled through the use of a dongle. Transparent at a software level, by the use of this technology, the system is able to calibrate the entire channel timing information for those connected modules, and operate as one multichannel digitizer.

The number of modules that can be connected in this way is limited due to the added jitter and distortion to the ADC clock signal as it is cascaded through the multiple clock circuits. With a maximum bank of 28 channels at 1 GSa/s, or 20 channels at 2 GSa/s, only three externally synchronised banks with shared reference clock and trigger signals would be required to create the example system of 50 channels, of 8-bit acquisition, at 2 GSa/s.

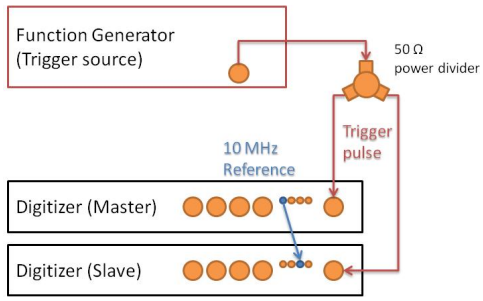

Figure 3: Block diagram of the hybrid external synchronisation scheme, where a 10 MHz reference clock is propagated from a master digitizer to a slave module.

PXI Synchronisation

PXI, or the PCI eXtension for Instrumentation is a development of the industrial computer standard CompactPCI, that includes special consideration for module synchronisation through backplane connections. This standard is designed specifically for measurement and automation applications, so synchronisation is not limited to only data acquisition cards, but also to the rest of the system that may include switches, actuators and other low speed devices.

The PXI backplane includes a common 10 MHz clock, a Star trigger topology and 8 shared, parallel trigger lines. The 10 MHz clock source and the Star trigger are comprised of matched length paths fanned out to every slot in the chassis, resulting in bounded, low skew synchronization resources for all modules. Also, the introduction of a "System Timing Module" allows both organized control of the Star trigger lines as well as an optional and higher quality source for the 10 MHz clock.

It's clear that by using these synchronisation resources, a scheme that is similar to external synchronisation method previously presented can be set up, without the need for external connections.

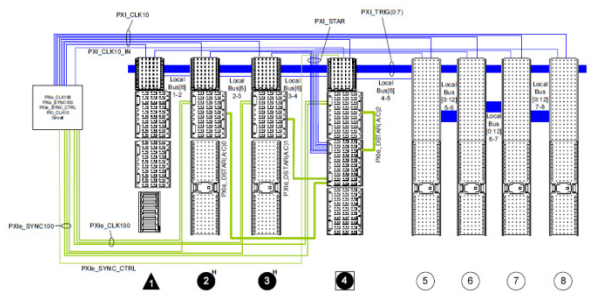

Figure 4: Block diagram of PXIe clock and trigger bus.

With the introduction of the PCI Express® high-speed serial bus, the PXI Systems Alliance [3] developed the PXI Express (PXIe) standard, to include not only a 10 MHz clock, but also a 100 MHz differential reference. It also added new unidirectional differential Star Trigger pairs with even. The new differential Star Triggers also

allow the possibility of providing higher speed reference clocks directly to select modules.

Due to the targeted applications, and size and power constraints of PXI and PXIe, typical high-speed digitizers will only achieve 1 or 2 channels at 2 GSa/s in a single peripheral slot. As such, to create a 50 channel, 2 GSa/s acquisition system using this method will require at least two 18-slot PXI or PXIe systems with shared reference clock and trigger signals, possibly requiring System Timing Modules for the highest accuracy, with individual machine states set through software.

AXIe Synchronisation

As the PXI standard was designed as an instrumentation extension on the PCI standard, so AXIe (AdvancedTCA® Extensions for Instrumentation and Test) is an extension for instrumentation based on the AdvancedTCA® standard. The AXIe standards consortium defined an initial base architecture in June 2010[4], see figure 5. The PCI Express® 100 MHz reference clock (FCLK) is distributed from the AXIe system slot to all of the other slots. FCLK is the low-jitter fabric clock. Usually provided by the PC for clocking the PCIe communications fabric, the FCLK fabric includes active buffers to fan-out the clock as individual, point-to-point differential pairs.

Three star fabrics provide additional 100 MHz, synchronisation and trigger. CLK100, the instrumentation clock, distributes a differential 100 MHZ clock from the system slot to the instrument slots through a backplane star. The SYNC star distributes a differential trigger signal from the system slot to the instrument slots. The STRIG star carries bi-directional trigger signals between the system slot and the instrument slots.

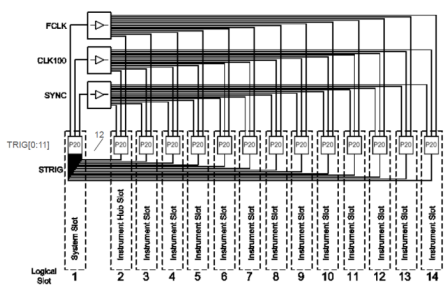

Figure 5: Block diagram of AXIe backplane clock and trigger interface.

The AXIe Trigger Bus, TRIG[0-11], made up of 12 MLVDS trigger pairs bused across all of the slots on an AXIe backplane. In addition to this synchronisation fabric, the AXIe local bus provides short differential signal pairs between adjacent AXIe slots, excluding the system slot. These allow very fast communication between processors in adjacent slots at Gigabit per second rates. A backplane synchronisation can easily be implemented using the combination of backplane reference clock and star trigger. By using the high-speed LVDS pairs of the AXIe local bus, it is possible to extend the synchronisation performance of an AXIe-based instrumentation system, to levels approaching that of a proprietary hardware synchronization scheme.

With its dimensions of 322.75mm x 30.48mm x 280 mm, and over 200W per slot, a digitizer based around the AXIe standard provides at least 4 times the resources of PXIe. An AXIe digitizer providing 2 GSa/s performance could have at least 8 channels per module. A 50 channel system built around an 8-channel unit would require the synchronisation of 7 cards, and a 14-slot AXIe chassis (supported by the AXIe standard as in figure 5) could contain 112 synchronous channels in a 19" rack.

CONCLUSIONS

As test applications continue to require higher and higher speed acquisition along with the need of multiple synchronous channels, new technologies are being produced to solve these unique challenges. Modular devices are viable options for high channel count acquisition systems requiring new levels of performance and the newest modular platforms are beginning to provide the common infrastructure to modular product developers for these applications.

Various schemes exist that allow the sampling clocks of all the ADC components in the system to be synchronous, with some fixed delay between channels. These delays are due to factors such as delay lines, signal path lengths and cable lengths. These path length delays however are often fixed and stable, in a controlled laboratory environment, and as such can be calibrated for.

The trigger point T_0 must be propagated to all modules. This too brings with it the challenges of propagation of a fast signal within the system, especially over extended distances.Finally the machine states of the individual digitizers may need to be synchronized, so that the system behaviour can be controlled and partial signal loss avoided.

Hardware standards today offer system level synchronisation based on backplane clock and trigger fabrics that allow us to simplify the task within a system.

The AXIe (AdvancedTCA® Extensions for Instrumentation and Test) standard provides a number of clock, trigger, synchronization and communications fabrics that can be used to develop a flexible and robust system level synchronization.

REFERENCES

[1] S. Marrone, *et al.* "A low background neutron flux monitor for the n TOF facility at CERN", Nuclear Instruments and Methods in Physics Research A 517 (2004) 389–398

[2] Y. Maumary, "Creating Synchronous High-Frequency Sampling Across Multiple Digitizers", Agilent Measurement Journal 2008, No. 5

[3] Website www.pxisa.org

[4] Website www.axiestandard.org