PHASE DETECTION ELECTRONICS FOR CLIC*

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Abstract

The Compact Linear Collider (CLIC) requires very tight RF phase synchronisation in order to preserve high luminosity. The electronics required for processing the signals delivered from the phase pick-ups present a significant challenge. This paper discusses the strategy adopted to achieve a sufficiently accurate measurement of the phase. Performance measurements performed in the lab of some of the sub-systems are also presented.

INTRODUCTION

The Compact Linear Collider requires a very tight synchronisation between its main and drive beams. As devices in the beam generation scheme are likely to introduce beam phase errors exceeding the tolerance of the machine by far, measurement and correction of those errors are necessary. To preserve high luminosity in the machine, the phase errors between the two beams must be below 46 fs (0.2 ° at 12 GHz) at the point of energy transfer. The measurement and correction, via feed-forward, of errors must be accurate up to the bandwidth of the structures, expected to be around 50 MHz. The combination of precision and bandwidth requirements makes this a challenging task on the electronics side. The budget allocated to the measurement side is 0.1 °. The bandwidth should be larger than the required 50 MHz for the full system; 100 MHz is aimed for [1].

PHASE REFERENCES AND PICK-UPS

Phase References

Laser based timing distribution systems have made a lot of progress as they are being developed for free-electron laser facilities. At the present time they can achieve femtosecond level stability over distances of about a kilometre [2]. Their extension to a CLIC-size machine (25 km) remains to be proven. Due to the layout of CLIC, there remains an option of an entirely local system. The main-beams are generated at the centre of the complex, and then transported outwards to the beginnings of the linacs. The main beam phase can therefore be picked up on the way out and compared to a precision local oscillator (scf. Fig.1). Correct time must then be kept for up to 160 µs. Oscillators with an integrated phase jitter of around 5 fs have been purchased.

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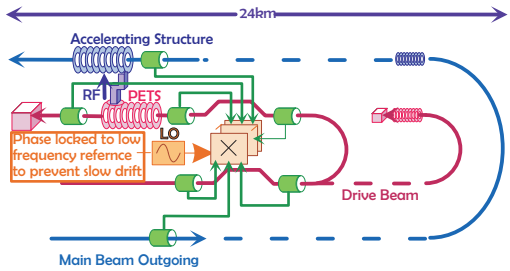

Figure 1: Concept of CLIC phase correction.

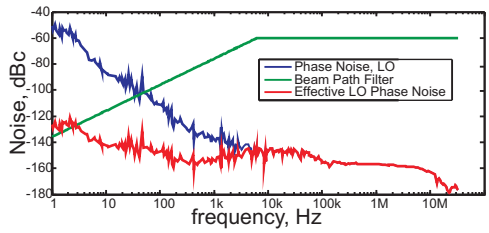

Figure 2: Local oscillator performance.

Pick-ups

Beam phase pick-ups have been designed and are being constructed. The pick-ups need to provide signals with sufficient resolution for the measurement requirement. In addition, the pick-up must present very low coupling impedance to the beam and reject any RF noise that might travel down the beam pipe [3].

DETECTION ELECTRONICS

High Frequency Phase Detection

The performance of detection electronics is limited by both device non-linearity and noise. Device non-linearity can cause disastrous degradation of performance as an amplitude modulation of the input signal is converted into a phase modulation. Device non-linearity decreases with input amplitude, whereas the signal-to-noise ratio gets worse. By splitting the input signal and using several detection devices, a noise reduction by the square-root of the number of devices is achieved. In a detection scheme where the 12 GHz signals are mixed directly to baseband, measurements indicate that 8 devices are sufficient to ensure that these two effects can be adequately reduced for an incoming signal with a 1% amplitude modulation. Since the output of the phase detection mixers is proportional to the incoming signal amplitude, this amplitude must also be detected and

taken into account. A similar scheme of device parallelisation will be used with power detection diodes to ensure adequate noise performance.

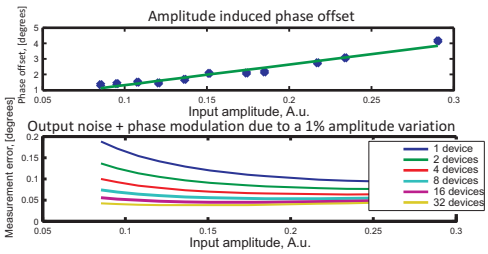

Figure 3: Amplitude induced phase modulation and noise.

High Frequency Board Layout Considerations

In order to achieve the required performance attention must be paid to the layout on the high frequency electronics board. The signal splitting required for device parallelisation is implemented directly in microstrip on a high frequency substrate. This avoids the use of external splitters where small changes in interconnects may yield unacceptable signal errors. Due to the narrow bandwidth required with respect to the 12 GHz centre frequency, splitters built as single stage Wilkinsons are sufficient. Simulations of the splitters with HFSS, using the expected manufacturing tolerances, indicate that they will perform to better than the required level. The boards are currently in production. The mixers that make up the phase detectors may however present sufficiently different phase condition at the inputs that not all devices are close enough to the 90 ° LO-RF difference required for efficient detection. If this is the case, a very simple phase trimmer that permits a phase shift of up to 15 ° while leaving the amplitude basically unchanged could be used and has been investigated. It consists of a small copper plunger which capacitively couples to the LO traces leading up to each mixer. A prototype was tested in the lab and showed promising performance.

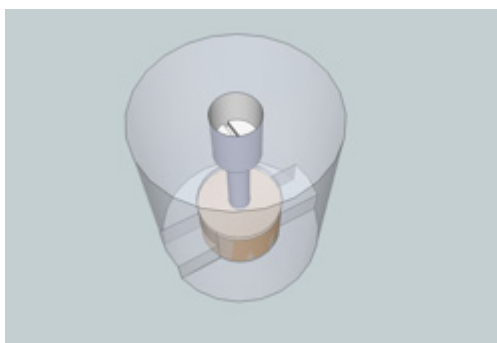

Figure 4: Capacitively coupled phase trimmer.

Baseband Signal Processing

Because of the short time interval (70 ns) between phase detection and correction, signal digitisation and digital processing will potentially introduce too large latencies. An analogue baseband processing board is therefore being investigated. Because the application requires only a limited amplitude and phase range, the functions to be implemented remain achievable. In terms of the detected amplitude proportional phase signal and the power signal we must compute: $\phi(t) = \frac{A\phi(t)}{\sqrt{P(t)}}$. Since we are only interested in a very limited input power range, a polynomial approximation of $\frac{1}{\sqrt{P(t)}}$ can be used. In a range of ±10% power variation the error between this function and its second order polynomial approximation is below 0.12‰, which is better than sufficient. To implement this second order polynomial, as well as the multiplication with the phase signal, high frequency analogue multipliers are used. These multipliers have quite bad input and output offsets (75 mV) as well as gain errors of 9%, both of which are temperature dependent. It is therefore necessary to implement a calibration function for this board. Comparators with 10 µV input offset can be found. Likewise, very precise voltage references and digital to analogue converters are available. Two gains and two offsets must be set at the appropriate values in order to implement the correct function. By using four widely spaced input set-points and adjusting the voltage value for the gain or offset associated with each one until the output value matches the expected one, the board can be very well calibrated. The calibration procedure cycles through the four until none of them changes by more than 10 µV in the same iteration. This procedure converges in 17 iterations or less when simulating 10k different random starting values. The output error after calibration in the ±10% power variation range is less than 48 µV, corresponding to $4.8\ 10^{-4}$ °. With the hand-built and hand-calibrated prototype a residual error of 2‰ (0.02 °) could be obtained. A bandwidth of ~150 MHz was achieved, and the output noise was 300 µV, corresponding to 0.003 °. The calibration processor will also monitor the signal output during the part of the cycle when the beam is not present for deviations from the expected output with zero input. Any drifts should therefore be detected as they occur, and a recalibration can be initiated.

BEAM TESTS

After the phase pick-ups have been produced and tested in the lab, they will be delivered to CERN for beam tests in the CLIC Test Facility 3 (CTF3). In the first stage the pick-ups themselves and the electronics will be verified. To achieve this, three monitors will be installed back to back in the linac to ensure identical beam conditions. The outputs of all three monitors will then be compared to each other. In a later stage, feed-forward correction will be tested using fast kickers.

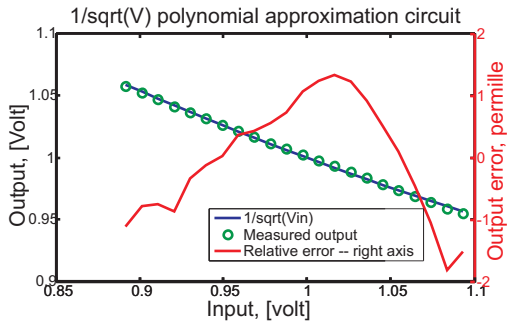

Figure 5: Analogue processor measurements.

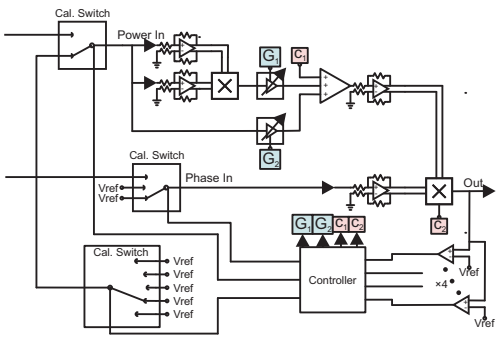

Figure 6: Analogue processing board with automatic calibration.

System Considerations

The signals coming from the phase pick-ups must at all times remain close to the nominal values for phase and amplitude, since only under these conditions accurate measurements can be made. The average beam phase and amplitude will therefore be continuously monitored, and their values adjusted as needed to adapt to slow drifts that may occur in the machine. Feedback paths are shown in dashed red lines in Figure 7. This is particularly important for the system that will be installed for beam tests in CTF3. This machine generates a drive beam in a similar manner as planned for CLIC. However, due chiefly to non-optimal RF power devices in the linac, the beam quality is generally poorer than can be expected in CLIC. In particular, the beam current and phase can be expected to suffer from slow drifts.

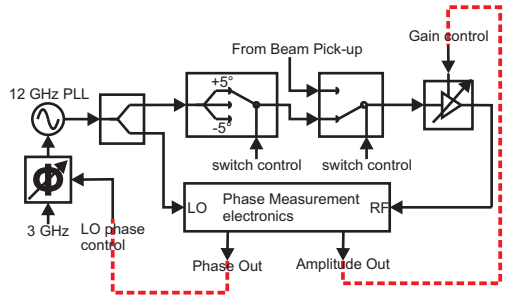

Figure 7: Phase measurement system layout.

CONCLUSIONS

The electronics required for the CLIC phase feed-forward correction system has been designed and simulated. Prototypes of some subsystems have been built and measured in the lab. The high-frequency boards are in production and nearing delivery. Upon arrival their performance will be verified in the lab. An automatic calibration system for the analogue processing board has been conceived. Design and production of this board will follow. System design has begun in preparation for beam tests in CTF3.

REFERENCES

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