PRELIMINARY DESIGN OF AN INDUCTIVE ADDER FOR CLIC DAMPING RINGS

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Abstract

The Compact Linear Collider (CLIC) study is exploring the scheme for an electron-positron collider with high luminosity and a nominal centre-of-mass energy of 3 TeV. The CLIC damping rings will produce ultra-low emittance beam, with high bunch charge, necessary for the luminosity performance of the collider. To limit the beam emittance blow-up due to oscillations, the pulse power modulators for the damping rings kickers must provide extremely flat, high-voltage, pulses: specifications call for a 160 ns duration flattop of 12.5 kV, 250 A, with a combined ripple and droop of not more than ±0.02 %. A solid-state modulator, the inductive adder, is a very promising approach to meeting the demanding specifications; this topology allows the use of both digital and analogue modulation. To effectively use modulation techniques to achieve such low ripple and droop requires an in-depth knowledge of the behaviour of the solid-state switching components and their gate drivers, as well as a good understanding of the overall circuit behaviour. This paper describes the initial design of the inductive adder.

INTRODUCTION

High-energy e+e- colliders, such as CLIC [1], will be needed to help unravel the TeV physics unveiled by the LHC. They would provide very clean experimental environments and democratic production of all particles within the accessible energy range.

Table 1. PDR & DR Kicker Specifications

Parameter	PDR	DR
Field rise and fall times (ns)	700	1000
Pulse flat-top duration (ns)	160	160
Pulse flat-top reproducibility	$\pm 1 \times 10^{-4}$	$\pm 1 \times 10^{-4}$
Flat-top stability, at injection	$\pm 2 \times 10^{-2}$	$\pm 2 \times 10^{-3}$
Flat-top stability, at extraction	$\pm 2 \times 10^{-3}$	$\pm 2 \times 10^{-4}$
Injection field inhomogeneity (%)	±0.1[A]	±0.1[A]
Extraction field inhomogeneity (%)	±0.1[A]	±0.01[B]
Repetition rate (Hz)	50	50
Stripline and load impedance (Ω)	50	50
Pulse voltage per stripline (kV)	±17	±12.5
Stripline pulse current (A)	±340	±250

[A]Over 3.5 mm radius [B]Over 1 mm radius

To achieve high luminosity at the Interaction Point (IP), it is crucial that the beams have very low transverse emittance: the Pre-Damping Ring (PDR) and Damping Ring (DR) "cool" the beam to an extremely low emittance in all three dimensions. The PDR is required to decouple the wide aperture requirements, for the incoming positron beam, from the final emittance requirements of the main linac. The design parameters of the PDR and DR are dictated by target performance of the collider, the injected beam characteristics or compatibility with the downstream system parameters: the emittances of the positrons must be damped by several orders of magnitude [2].

Kickers are required to inject beam into and extract beam from the PDRs and DRs. Jitter in the magnitude of the kick waveform translates into beam jitter at the IP [2]. Thus the PDR and DR kickers, in particularly the DR extraction kicker, must have a very small magnitude of jitter as well as low longitudinal and transverse beam coupling impedances. Table 1 shows the specifications for the PDR and DR kickers [3]: the specified stabilities include all sources of contributions such as ripple and droop. The values in Table 1 may be refined as the optics design progresses. Striplines will be used for the kicker elements in order to meet the specifications for the beam coupling impedances [4, 5].

THE INDUCTIVE ADDER

A review of literature of existing pulse generators has been carried out and an inductive adder (Fig. 1) has been selected as a very promising means of achieving the specifications for the PDR and DR extraction kickers [6]. The inductive adder is a solid-state modulator, capable of providing relatively short and precise pulses. With a proper design of the adder it may be possible to meet the ripple and droop requirements of the PDR kicker [7]. However, digital and analogue modulation of the output pulse may be required to reach the specifications of the DR kicker. A method to measure the output ripple of the pulse generator will also require significant development.

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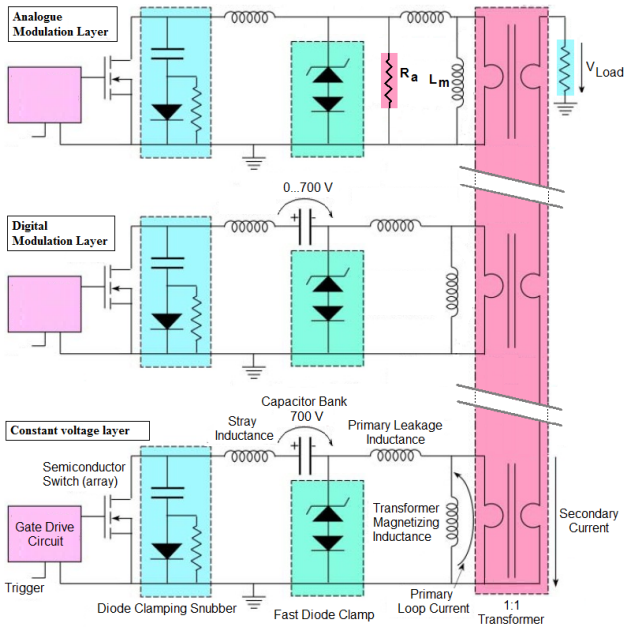

Figure 1: Schematic of an inductive adder with a constant voltage layer, a digital modulation layer and an analogue modulation layer.

SELECTION OF THE MAIN COMPONENTS

Semiconductor Switches

MOSFETs have been selected as the first candidate switch for the PDR and DR kickers, because they have many advantages over other switches. Switching transitions of MOSFETs are very fast, which allows short duration pulses. In addition MOSFETs are easy to control and they have low time jitter, usually in the order of sub-nanoseconds. Fast power MOSFETs are also available for operation in their linear region, which is required if analogue modulation techniques are used.

The operating voltage of the switches defines the number of layers in the adder stack. MOSFETs are available with voltage rating of up to 1.2 kV: for long-term reliability, while minimizing the number of layers, the solid-state switches will be operated at 60% to 70% of their voltage rating. Implementing the 12.5 kV DR kicker modulator with switches with an operating voltage of 700 V will require a minimum of 18 layers.

Capacitors

The layers of the inductive adder must be designed to have very small loop inductances, which may require custom-made capacitors. The required capacitance per layer, to directly achieve a given load voltage droop, without using modulation techniques, is proportional to the number of layers [6]. For a load with 160 ns wide flat-top pulses of 12.5 kV and 250 A, allowing 0.02% (2.5 V) for droop requirements (the other 0.02% is an allowance for ripple), and an inductive adder consisting of 18 layers, the required capacitance per layer is 320 µF. This includes an allowance for a magnetizing current of 30 A.

Magnetic Cores

The maximum output pulse-width of the inductive adder is limited by the saturation of the transformer core. The minimum required cross-sectional area (CSA) of the core is inversely proportional to the available flux-density swing [6]: the core can be biased to increase the available swing and therefore reduce the required CSA.

To minimize load voltage rise-time, eddy currents in the cores must be controlled: tape-wound cores must have adequate insulation to avoid breakdown between magnetic laminations. For a toroidal core it can be shown that the interlaminar voltage, V_{il}, is given by [7]:

$$V_{il} = \frac{A_{il}}{2 \cdot \pi \cdot r} \cdot N \cdot \mu_0 \cdot \left(i \cdot \frac{d\mu_r}{dt} + \mu_r \cdot \frac{di}{dt} \right)$$

where A_{il} is the interlaminar cross-sectional area, r is the radius of interest, N is the number of turns and i is current. For a non-magnetic interlaminar insulation, the first term in parentheses is equal to zero. The above equation shows that the interlaminar voltage is highest near to the inside radius of the core.

Temperature effects can have a significant influence upon the magnetic parameters of the transformer core and this must be carefully considered at the design stage [8].

Dimensioning of Stack Secondary Winding

The secondary winding of the adder stack will be a single turn conducting rod. The output impedance of the stack will be matched to the impedance of the load to avoid reflections. The primary leakage inductance of the transformer must be taken into consideration in defining the dimensions of the secondary conductor and hence its inductance and capacitance. Equations for approximately dimensioning the inductive adder cell have been published [9].

Design Steps

The design of the dimensions of the inductive adder is an iterative process. The process can be carried out as follows: (a) choose the type of semiconductor switches, their voltage rating and operating voltage; (b) calculate the number of primary layers, including redundancy; (c) estimate the value of capacitance per layer; (d) determine the minimum CSA of the magnetic core – including a suitable safety margin; (e) determine the dimensions of the coaxial transformer structure.

Primary capacitors need to be located very close to the primary winding to keep the loop inductance low. If a large value of capacitance is required per layer, the outer diameter of the transformer core can be selected to fit the

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capacitors in a circle around it. The minimum height of one layer is defined by the height of capacitors.

The space between the primary and secondary windings is filled with dielectric material: the outer and inner diameters of the dielectric are set by the insulation requirements of the output. Below 20 kV, air insulation may be sufficient [10]. The outer diameter of the secondary conductor is calculated based on equations of the inductance and capacitance of a coaxial transformer [9]. The value of leakage inductance may not be computed exactly at this point, hence dimensioning of the adder stack may require several iterative steps.

COMPENSATION OF DROOP

The ripple and droop requirement of the DR kicker is tighter than for any pulse power modulator found in the literature and various techniques are being studied to achieve the specifications. Fig. 2 shows simulation results with different capacitances per layer and with a passive and active analogue modulation layer. Without modulation 320 µF per layer is required to achieve the specified droop: with analogue modulation, the droop is within specification with a capacitance per layer of 40 µF [6]. For the prototype inductive adder it is proposed to use 80 µF per layer. A feed-forward compensation of known or predictable ripple components could also be applied with active droop cancellation: this will be investigated.

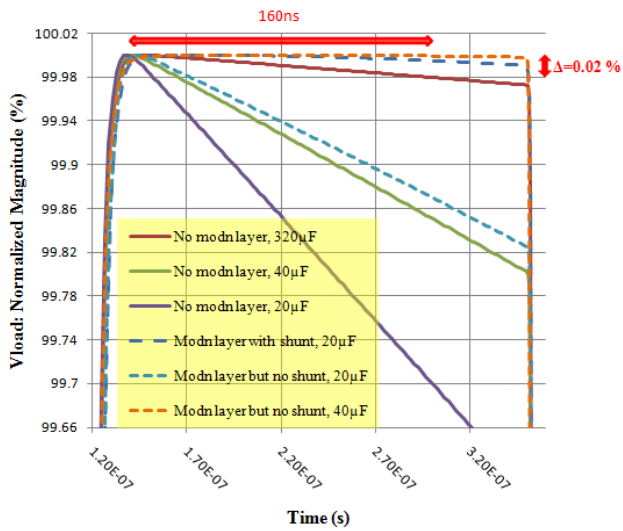

Figure 2: Simulation results for an inductive adder with different capacitances, with and without an analogue modulation layer.

CONCLUSIONS

The inductive adder is a promising means of reaching the very demanding specifications of the CLIC PDR and DR kicker modulators. New techniques are required for cancelling ripple and droop of the load pulse to achieve the desired flat-top ripple requirements. Preliminary circuit simulations of analogue modulation techniques confirm that this is a promising approach to meet the demanding specifications of the PDR and DR kickers. The prototype of the PDR and DR kickers requires very careful design of the adder stack as well as testing and qualifying of candidate components. Samples of components will be tested during 2011. The goal is to build the first prototype layer by the end of year 2011.

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