PRELIMINARY TESTING OF TPS TIMING SYSTEM

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Abstract

The Taiwan Photon Source timing system provides synchronization for electron gun, modulators of linac, pulse magnet power supplies, booster power supply ramp, bucket addressing of storage ring, diagnostic equipments, beamline gating signal for top-up injection. The timing system utilizes a central event generator to generate events and distribute them over optic fiber network, and decodes them at the event receivers. The system supports uplink functionality which will be used for the fast interlock system to distribute signals like beam dump and post-mortem trigger. The timing system has now been in operation for linac of TPS. About time stability (jitter), response time, sequence control and etc. are critical parameters for timing system. This paper presents results of parameter measurements for the timing system of TPS.

INTRODUCTION

The TPS is the latest generation synchrotron light source. Event based timing system is applied for TPS due to its high performance and flexibility which has been already verified in many advanced light sources [1]. Negotiate with the vendor to implement the EVG and EVR in the desired 6U cPCI form factor was started from 2008. The first lot of EVG and EVR modules were received in later 2010. Efforts to setup the test system were done in the first quarter of 2011. The pre-delivery system already applied for the TPS 150 MeV linear accelerator commissioning and acceptance during the second quarter of 2011 with highly success. The system design and check are on going. Preliminary test of functionality and system performance will be summary in this report.

TIMING SYSTEM

The TPS timing system is an event based system. A central event generator (EVG) generates events from an internal sequencer and external sources [2]. These events are distributed over optic fiber links to multiple event receivers (EVRs) [3]. The EVRs, which are located in the control system interface layer, decode the events referred to as hardware triggers or software interrupts. For the linac, the decoded events are further encoded by a gun transmitter and sent over a fiber link to the gun high voltage platform. The external event sources include PPS signal which is locked to GPS, AC mains 60 Hz trigger, post-mortem trigger after beam loss and machine protection system trip. The event clock is derived from the 499.654 MHz master oscillator so that it is locked to change in the RF frequency. The structure is shown in Fig. 1. The master oscillator can be used as an external reference from a GPS disciplined Rubidium 10 MHz clock. Fig. 2 shows TPS timing modules include EVG, EVR, EVRTG and linac gun trigger receiver.

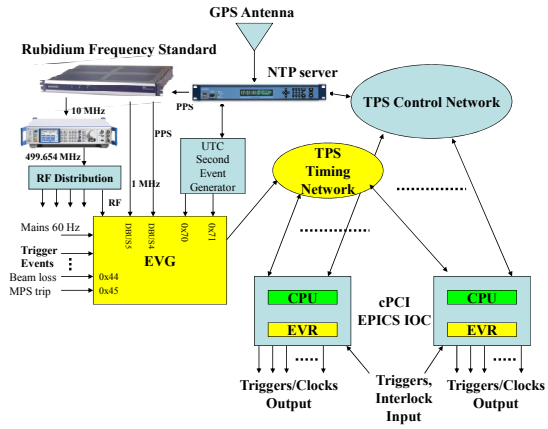


Figure 1: Block diagram of the TPS event system.

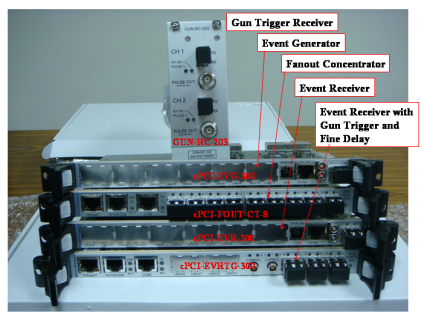


Figure 2: TPS timing modules.

Event Generator

The cPCI-EVG-300 generates event frames consisting of an 8-bit event code and an 8-bit distributed data bus, at a rate of 125 MEvents/sec. Events can originate from several sources including: eight external trigger events, a sequence RAM, software events and events received from an upstream event generator. Events from different sources have different priorities which are resolved in a priority encoder. A block of RAM is used to store a sequence of events. In cPCI-EVG-300 the input RF clock (499.654 MHz) is divided by 4 to generate the event clock for the TPS timing system. Therefore, the resolution of timing event is 8 ns. The cPCI-EVG-300 is realized as a 6 U CompactPCI (cPCI) module.

Event Receiver

There are two versions of 6U cPCI EVR available, cPCI-EVR-300 and cPCI-EVRTG-300. The cPCI-EVR-300 recovers the event clock signal from the event stream and splits the event frame into the 8-bit event code and

the 8-bit distributed data bus. The decoded events are mapped through RAM on to: trigger twelve pulse generators with programmable delay and width (32-bit prescaler from the event clock, 32-bit delay and 32-bit width) or set/reset twelve pulse generators. The cPCI-EVR-300 provides 3 programmable 16bit prescaler from the event clock. The twelve front panel outputs can be mapped to any output such as each pulse generator output, prescaler and distributed bus bit. The cPCI-EVRTG-300 has eight channels; it includes two UNIV I/O slots support up to four various output and input, two LVPECL outputs and two SFP outputs. The cPCI-EVRTG-300 have jitter cleaner to achieve jitter same as VME-EVR-230RF (a few psec).

The cPCI-EVRTG-300 has two SFP ports that can generate modulated optical signals that can be decoded by the GUN-RC-203 for linac gun driver trigger. The two SFP ports share an external inhibit signal. The GUN-RC-203 consists of two channels to provide single-bunch and multi-bunch injection respectively. It is realized as a cPCI-EVRTG-300 in the linac timing crate and a GUN-RC-203 placed on the gun HV platform. The fine programmable delay is also available and allowed to adjust the triggering position with a resolution of 10 ps over a range of 10 ns. The GUN-TX-203 mode has been designed to operate output pulse delayed by 1/4, 2/4 and 3/4 event clock period (~2, 4, 6 ns). The new module GUN-RC-300 will support arbitrary pattern.

Distribution

The timing distribution network delivers the event stream using OM3 multi-mode fiber. The network is structured as a three-level multi-star topology using 28 fan-out concentrator modules. EVG to multiple EVRs is arranged by using fibers of equal lengths about 350 m.

EVENT GENERATION

The TPS storage ring has 864 buckets with revolution frequency of 578.303 kHz, and the booster 828 buckets and a revolution frequency of 603.445 kHz. The coincidence of the SR and booster revolution determines a frequency for the coincidence clock of 25.14 kHz. The event clock is used for counting through the EVG sequence RAM, which provide 8 ns resolution. The coincidence clock synchronizes the machine repetition rate which is derivate from AC mains frequency and used to reset the start of the sequence, thereby locking the cycles of all accelerators. Event entries are placed in the sequence RAM to generate the necessary sequence of triggers to accelerate the electrons through the linac and booster into the SR. Additional events provide trigger of the TPS diagnostics, gating signals for beamline in top-up operation, and beam loss post-mortem.

SOFTWARE

The timing system integrates into the TPS EPICS control environment. The EVG configuration pages define the options of cPCI-EVG-300. These include configuration of the EVG operating mode, selection of RF and AC divider, definition of multiplexed counter, optional transmission of software events, enable of event trigger inputs and specify event code and timestamp into the sequence RAMs. The EVR configuration pages configure the options for the cPCI-EVR-300, such as pulse delay, width and polarity, front panel output assignments and distributed bus enable and event decoding mapping RAMs. Applications to control the timing system are built with the usual EPICS tools for databases and EDM for user interface. The EVG/EVR configuration GUI is shown in Fig. 3.

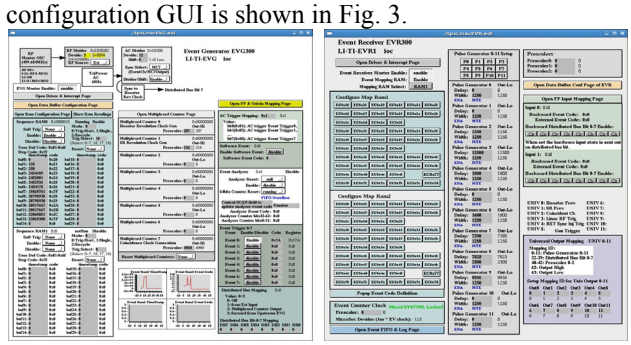


Figure 3: EVG/EVR configuration GUI.

CURRENT STATUS

The first lot of EVG/EVR modules was received in December 2010. Setup of the test system has been started from February 2011.

Timing for the 150 MeV Linac System

The timing distribution network delivers the event stream using OM3 multi-mode fiber. The network is structure Configuration tools for the EVG/EVRs were implemented. Timing for the linac RF trigger and e-gun trigger are ready for operation which is required for the commissioning of the TPS 150 MeV linac started from April, 2011. Prototype of timing summary control page is shown in Fig. 4.

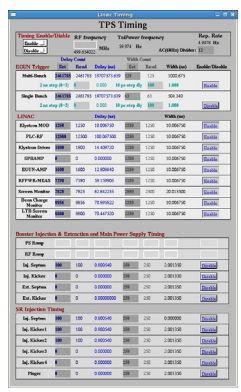
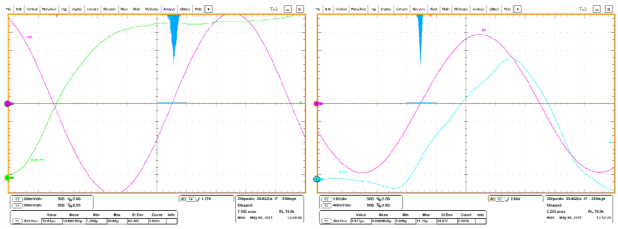


Figure 4: Prototype of timing summary control page.

The timing jitter of the installed prototype system of the decoded event with TTL output respect to the RF clock is around 20 ps for the cPCI-EVR-300 as shown in Fig. 5 (a). The jitter of the beam relative to the RF source is less than 10 ps for the cPCI-EVRTG-300 with GUN-RC-203 module as shown in Fig. 5(b).



(a) (b)

Figure 5: (a) Jitter of the cPCI-EVR-300 TTL output relative to the RF clock and (b) Jitter of the beam relative to the RF clock. The beam is triggered by combination of the cPCI-EVRTG-300 and GUN-RC-203 trigger module.

Timing Measurement

Layout for response time measurement is shown in Fig. 6. The EVG issues an MPS-TRIP event stimulated by a trigger on the universal input module (UNIV-TTLIN). The EVR receives the event stream, decodes MPS-TRIP event and outputs them as 1 µs pulses on universal output module (UNIV-TTL). The estimated summing delays between the MPS-TRIP trigger pulse and the EVR decoded event is 342 ns, with a 10 meter fiber (~50 ns) patch taken into account.

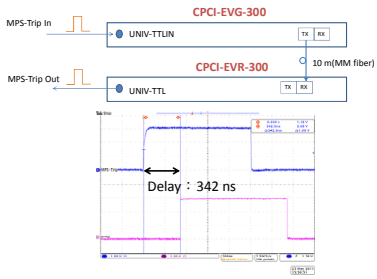


Figure 6: Delay between the trigger input to EVG and output from EVR with a short fiber link.

Measurement of the global response time for the TPS timing systems uplink and downlink is presented in Fig. 7. This event code 0x45 is used for indication of MPS-TRIP event. The event is stimulated by an external trigger produced by an EVR2. According to the oscilloscope pattern the EVR2 transmitted event by MPS-TRIP trigger and EVR1 decoded event pulse are shifted with respect to each other by 2.45 µs. The global response time is 4.42 µs which consists of EVG, EVR1, EVR2, three fan-out concentrators processing times and propagation delay time along timing system fiber network (Fig. 7).

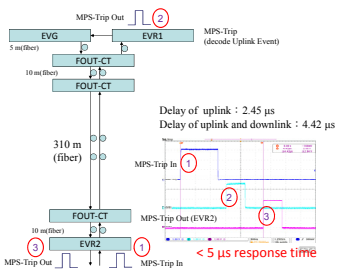


Figure 7: Timing measurement of uplink and downlink with 310 m fiber and three stages of fan-out distributor.

Sequence Control

The Matlab is planned for global machine sequence control for the TPS project. Sequence RAM control of the injection scenario has been tested by Matlab script running in control console over Ethernet to change the sequence RAM of EVG in the timing master EPICS IOC. The Matlab test script detects sequence RAM interrupt and replaces sequence RAM contents. Fig. 8 shows the process time executed by Matlab test script is around a few msec. The TPS will be operated in 3 Hz repetition rate. The booster power supply ramping waveform is 3Hz sinusoidal wave and T-ZERO defined at 0 msec. The storage ring extraction time is T-ZERO+166.66 msec. There are more than 100 msec time window to do sequence RAM management. The process time is much less than 100 msec. So using Matlab script for sequence RAM control is sufficient. The Matlab script will be run in the timing master for sequence RAM control in machine operation. All parameters for the machine operation modes and parameters will be designed as specific EPICS PV, such as bucket address, repeat cycle, top-up injection, decay mode and etc.

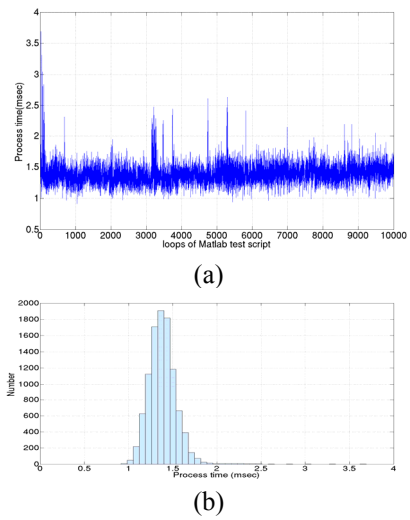


Figure 8: (a) Process time of the Matlab script to change content of sequence RAM by over Ethernet for 10000 loops. (b) Histogram of (a).

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REFERENCE

[1] Y. Chernousko, et al., “Review of the Diamond Light Source Timing System”, Proc. of RuPAC-2010, Protvino, Russia. pp. 144-146.

[2] Micro-Research Finland Oy, “Event Generator”, Document: EVG-MRM-0003, 4 January 2011.

[3] Micro-Research Finland Oy, “Event Receiver – Technical Reference”, Document: EVR-MRM-003, 7 April 2011.