UPGRADE OF THE ISIS SYNCHROTRON LOW POWER RF SYSTEM

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Abstract

The ISIS synchrotron at the Rutherford Appleton Laboratory in the UK now routinely uses a dual harmonic RF system to accelerate beam currents in excess of 230μA to run two target stations simultaneously. In order to give more stable control of the phase of the RF voltage at each of the fundamental (1RF) and second harmonic (2RF) cavities, changes have been made to the low power RF (LPRF) control systems. In addition to this a new FPGA based master oscillator (MO) has been commissioned for the first time, and further changes using digital technologies to replace other components of the LPRF system are to be investigated. This paper reports on the LPRF hardware commissioning.

INTRODUCTION

Much work has been reported previously [1] on the commissioning of the ISIS second harmonic (2RF) systems. Until the last year or so, the majority of effort has been spent on the high power systems, in particular the anode power supplies, and these systems are now operating reliably. This has allowed effort during the limited beam-time dedicated to ISIS machine development to be spent on further improvement of the LPRF system. This system controls the phase and amplitude of the accelerating voltages and of the tuning of all the ISIS synchrotron RF cavities. The existing LPRF control system is highlighted in Figure 1.

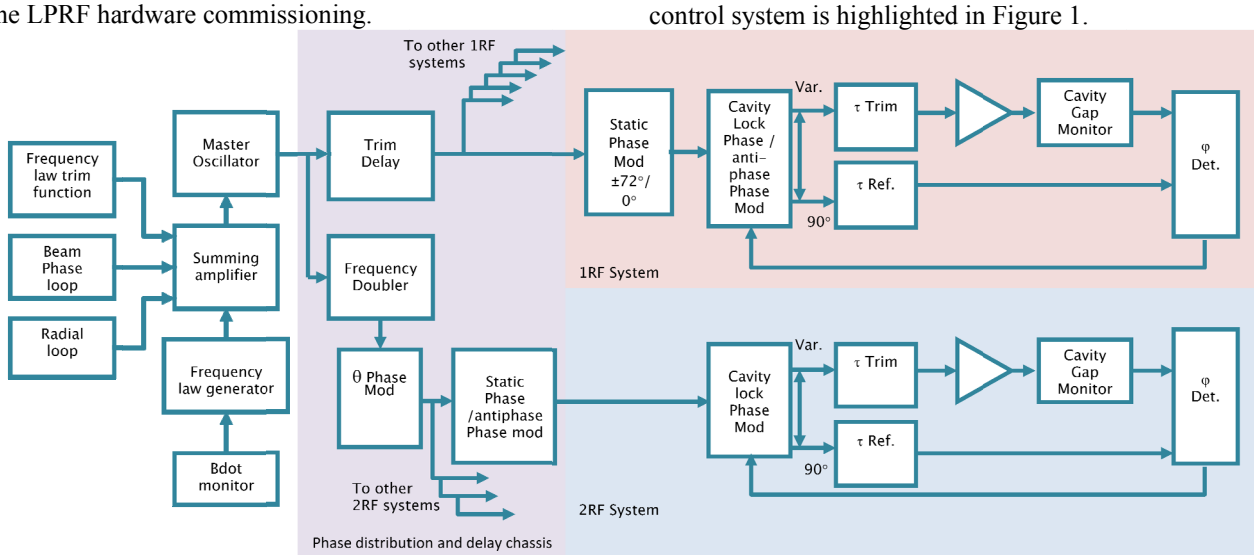

Figure 1: Schematic of the ISIS LPRF system.

IMPROVED 2RF PHASE CONTROL

Initial operation of the ISIS dual harmonic RF system gave poor control of the phase offset, θ, of the 2RF signal with respect to the 1RF signal. The value of θ measured on any particular 2RF system showed errors of up to 20° from the demanded phase. Greater control of the applied θ was achieved by closing a loop by comparing the phase of the measured gap voltage on one of the 2RF cavities with that of one of the 1RF cavities in a phase detector and applying the output of this phase detector as a correction to the demanded phase in the θ phase modulator. This gave increased stability of the θ phase. Currently only 2 out of the 4 2RF cavities are used during ISIS operational cycles, so to enable seamless switching between any of the 2RF cavities, the θ loop was modified to use the total accelerating gap voltages of the 1RF and 2RF systems. The system schematic for this configuration is shown in Figure 2. Operation in this configuration has helped to improve beam stability and allowed an increase in the ISIS accelerated beam intensity to operational levels of 230μA.

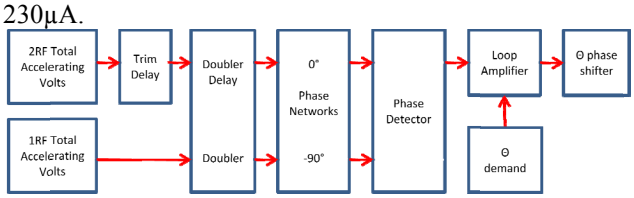

Figure 2: Closed loop for θ control.

RF CAVITY FEEDBACK

The recent success of the Low Output Impedance high power drive amplifier [2] inspired a design for closing an RF feedback loop around the intermediate and final stage high power drive amplifier on one of the ISIS 2RF systems. Tests were made using a modified version of the ISIS feed-forward beam compensation chassis, which allowed a feedback signal split from the cavity gap voltage monitor to summed with the drive signal, as shown in Figure 3.

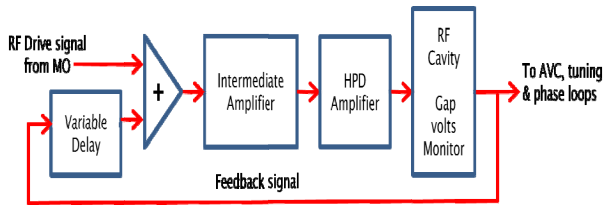

Figure 3: RF feedback system diagram.

The feedback signal was passed through a series of switchable delay lines in order to adjust the total loop delay to bring the feedback signal in anti-phase with the demand signal. The total measured delay through the signal cable and amplifiers was of the order of 570ns. As the top frequency of the ISIS 2RF sweep is 6.3MHz, this gave the smallest number cycles of to achieved antiphase at the summing amplifier was 4½. The delay was varied from 1.09µs at beam injection to 160ns at extraction and it was noted that the RF drive signal increased by 50% throughout the acceleration cycle, confirming that anti-phasing of the feedback signal had been correctly applied.

The loop gain was increased up to a value of around 2, beyond which oscillation of the cavity voltage occurred. This is thought to be due to a combination of the loop stability being limited by the rapid phase gradient that operation over 4.5 cycles imposes together with the introduction of rapidly varying transients in the feedback signal due to the delay line switching. However, even with this limited loop gain, tests with beam of 2.4×10^{13} protons showed a reduction in the oscillations on the cavity voltage envelope, as shown in Figure 4.

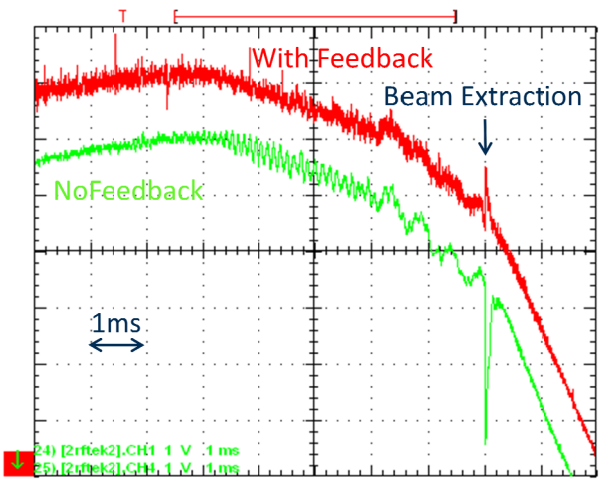

Figure 4: Gap voltage envelopes for RF feedback loop.

One can see the 8-9kHz beam induced oscillations on the envelope monitor signal that occur from 5-8ms in normal operation are reduced by the feedback loop, though more noise is seen on the signal, in addition to the large switching transients. Furthermore, the cavity gap-voltage transient at beam extraction appears to have dramatically reduced, due to a reduction of the effective cavity impedance. Since these tests were performed, a new cable has been laid to the cavity, reducing the total loop time by 200ns or so. This should enable the loop stability to be increased and the loop noise to be dramatically reduced. Further tests are to be carried out in the next available machine physics period.

DIGITAL MASTER OSCILLATOR

An FPGA based digital master oscillator [3] has been designed and is currently being commissioned which will provide the demand signal to each of the 10 (6 1RF and 4 2RF) accelerating RF cavities. Recent improvements to the coding on this device have included:

- Code restructuring, with Pipelining to achieve timing requirements on the Phase-Control data paths.
- Redesign the Phase Interpolator used in the dynamic switching of the Phase-AntiPhase control. Achieves a variable gradient proportional to the number of Delta P's specified.
- "On-the-fly" phase addition and subtraction.
- Changes to θ from a one-time download to an input from an external dynamically read digital interface.
- Common-mode noise filters were applied in-line from the Switched mode PSU's to reduce the frequency jitter on the MO unit to <1kHz.
- User-Interface modified to a synchronous architecture to improve reliability from user inputs.
- Modified the FLASH Memory interface for timing and control using the I2C bus, to provide reliable parametric data storage.
- PCB modifications required to the reset distribution system and general solder assembly quality issues.

The planned implementation of a UART for interactive PC control was not possible, due to the FPGA routing resources being heavily utilised. This would require an FPGA upgrade requirement for any future system development.

Initial commissioning has been performed with a single 1RF output from the digital MO used to replace the existing master oscillator signal input into the phase distribution chassis (as shown in figure 1). With the same input signal applied, the output 1RF sweep new MO produced a frequency sweep within 1kHz of that provided by the old unit, and allowed the stable operation of the 1RF and 2RF systems. Further work is now required to further integrate the new MO into the LPRF system, by using the new unit to provide the RF drive signal directly to each of the individual cavity LPRF systems, with the appropriate static phase offset applied for the position of the cavity, anti-phasing for augmentation of the level control loop dynamic range and θ phase shift for the 2RF cavities.

NEXT GENERATION LPRF

Recent effort on the LPRF systems has been concentrating on an "off-the-shelf" solution for test and development of new LPRF controls. A National Instruments FlexRIO FPGA module was purchased initially to implement a tuneable filter for trial use in the ISIS feed forward beam compensation system on the ISIS

second harmonic cavities. The FPGA module chosen was the PXI express based 7962R together with a 5781 adapter module, consisting of two 14 bit ADCs and two 16 bit DACs, which can be clocked at 100MHz.

The above system was used to develop and implement a digital filter with 40dB stop band attenuation and a passband bandwidth of 1MHz or so, around a centre frequency ranging from 2.6MHz to 6.3MHz. The centre frequency is changed by changing the filter coefficients 5 times throughout the 10ms ISIS acceleration cycle, in order to track the 2RF frequency component of the beam compensation signal before applying the filtered correction to the drive signal.

It soon became clear that the combination of the FlexRIO modules in conjunction with Labview FPGA development module would prove a rapid and simple means to implement new designs for other aspects of the LPRF controls. A simplified version of the ISIS master oscillator was produced which could be used to provide locked fundamental and second harmonic frequency signals with the appropriate θ phase offset, using a single analogue input from the ISIS frequency law generator summing amplifier. Whilst this is, admittedly, a simplified version of the digital master oscillator described in the previous section, it did take a fraction of the development time: around 6 months compared with the 3 years or so taken to develop the previous digital master oscillator. The current aim is to implement more and more sub-components of the LPRF system on the FlexRIO module.

A variable delay module has already been produced which can delay the digitised RF signal by a variable amount throughout the acceleration cycle. This will be used in the RF feedback loop tests in order to remove the delay line switching spikes in order to reduce the resultant oscillations on the feedback system. There are limitations to this approach: the minimum delay through the ADC, FPGA delay and summing module and DAC is of the order of 750ns. This is too large for a single RF cycle, and the feedback loop can only be applied over several RF cycles (especially at the top end of the 2RF sweep - 6.3MHz). However, much of this latent delay occurs in the output filtering of the DAC, and investigations are underway to reduce this.

The next component of the LPRF system to be implanted on these modules is an IQ demodulator which will form part of an IQ modulation loop. The final implementation will consist of the integration of these individual components. Each FlexRIO module should be capable of providing the drive signal to the intermediate amplifier of one RF system with the two ADC inputs to digitise the HPD grid volts and Cavity Gap volts signals. The second analogue output may be used to provide the cavity tuning current signal.

Earlier in 2011, a second FlexRIO module was purchased to investigate peer to peer data streaming on the PXI express chassis and timing synchronisation, which is expected to allow less than 10ps jitter between two separate FPGA clocks. Deployment of the two existing FlexRIO units together will allow tests with one unit replacing the Master Oscillator signal providing the existing frequency doubler and phasing chassis such that the ISIS RF systems can be run as they are at present. The second unit will be used to control an independent, but synchronised, RF signal to one system, with closed loop control of the amplitude and phase via the IQ modulation loop and of the cavity tuning current.

Should these tests succeed it would then be a relatively simple process to introduce more modules to each RF system, to provide each RF cavity with a synchronised local oscillator and IQ control and tuning loops, as shown in Figure 5.

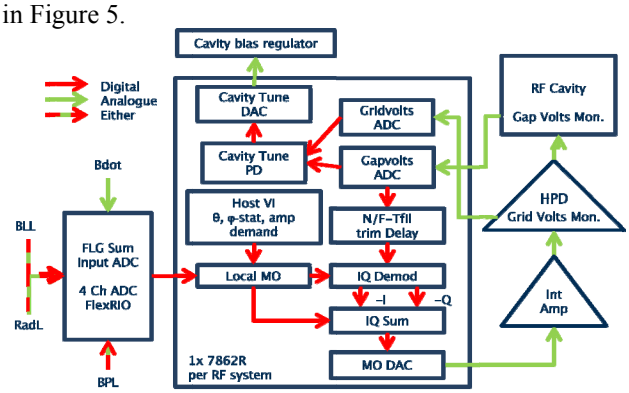

Figure 5: System diagram for a digital local oscillator.

CONCLUSIONS

The improvement of the existing ISIS LPRF system has been a continuous process. Improved control of the relative phasing of the 2RF cavities has been achieved. The initial tests of the closed feedback loop control of the RF cavity gap voltages proved very encouraging. If further loop stabilisation of this system can be achieved in the forthcoming machine development, this relatively simple and inexpensive approach could be easily applied to each RF cavity may yield much improved stability of the accelerating voltages. Damping the oscillations could then lead to a reduction in the mid-cycle beam losses that limit the ISIS beam intensity.

Whether or not the final implementation of the next digital LPRF system is a completely off the shelf solution remains to be seen, but the FlexRIO FPGA modules have proved successful in providing a rapidly deployable test-bench for the development of the modular components that will eventually such a system. The flexibility of both the reconfigurable FPGA devices, and the associated hardware interface modules should allow this new digital system to replace more and more of the functionality of the existing system in manageable stages.

REFERENCES

[1] A. Seville et al., "Progress on Dual Harmonic Acceleration on the ISIS Synchrotron", EPAC 2008.
[2] Y. Irie et al., "First Beam Experiments at ISIS with a Low Output-impedance Second Harmonic Cavity", these proceedings.
[3] C. Appelbee et al., "Digital Master Oscillator results for the ISIS Synchrotron", EPAC 2008.