COMPACT SOLID STATE RF-MODULES FOR DIRECT DRIVE RF-LINACS

R. Irsigler, M. Back, O. Heid, T. Hughes, Th. Kluge, J. Sirtl, Siemens AG, Erlangen, Germany
R. Baumgartner, M. Kaspar, K. Weidner, M. Zerb, Siemens AG, Munich Germany

Abstract

We present a modular RF power source concept based on solid state RF-modules with novel silicon carbide (SiC) transistors. The SiC power transistor has a very low input capacitance and was optimized for low gate resistance to enable fast switching in the RF range. It delivers a maximum pulsed drain current of 60 A. The transistor provides at 350 V and 150 MHz an output power of 5,6 kW with a gain of 15,8 dB. We have built very compact 75 x 90 mm ceramic amplifier modules using a planar interconnect technology (SIPLIT®) to connect the bare die transistors to the DCB substrate. The modules have a fully symmetric push-pull topology (circlotron) with four transistors in parallel in each leg. The RF-modules delivers at 324 MHz a maximum RF output power of 28 kW at 450 V supply voltage.

INTRODUCTION

High power RF-sources are key elements of linear accelerators that are used in numerous applications like particle physics, particle therapy and non-destructive testing. Our modular RF-source concept is based on solid state RF-modules with novel SiC transistors. The concept offers the perspective of lower cost, high integration, better thermal management, better reliability and reduced maintenance compared to traditional RF-source technology (e. g. Klystrons) [1]. It was already shown, that high pulsed RF power can be generated by operating many of these RF-modules in parallel on a power combiner cavity [2]. Our first version of the RF-module delivered at 150 MHz a pulsed RF output power in the range between 5 kW and 25 kW at supply voltages between 160V and 500V. We now present our next generation of solid state RF-modules using a further improved SiC transistor and an optimized substrate and assembly technology.

SIC POWER TRANSISTOR

SiC offers the advantage of larger bandgap (x3) and higher electron saturation velocity (x2) compared to standard silicon material. The high electric breakdown field strength (x10) allows higher doping levels and thinner layers in the channel and drift regions of the transistor which both lower the drain-source on-resistance $R_{ds(on)}$ (x1/100) and enables to build devices with higher blocking voltages (x10). The better thermal conductivity (x3) allows higher junction temperatures and higher power densities compared to their silicon counterparts. SiC power transistors are hence relatively small and have a low input capacitance which is a premise for fast switching in the RF range.

Our SiC transistor were designed and fabricated by SiCED (now Infineon). The distributed gate network on the SiC power transistor was optimized for low gate resistance. It is a lateral channel vertical junction field effect transistor (LC-vJFET). The total lateral chip size is 2,8 x 2,8 mm. The device has a input capacitance C_{iss} of about 600 pF, an internal gate resistance R_g of 0,3 Ω and a $R_{ds(on)}$ of 130 mΩ. It is a normally-on device with a pinch-off voltage of -17 V and a breakdown voltage of 1700V. A significant advantage of the SiC-vJFET is the fast and robust body diode that enables an operation without additional freewheeling diodes or circulators.

At low current levels, the transistor operates like an ideal current source providing a constant drain current independent of pulse length and drain voltage. However, at very high current levels, the drain current starts to degrade due to self-heating effects with increasing drain voltage and pulse length. This is shown in Fig. 2. The maximum pulsed drain saturation current of about 60 A is observed at about 40 V and degrades to about 38 A at 350 V. The mean drain saturation current at a gate voltage of 0V is also shown in Fig. 1 for different pulse lengths. While the mean current remains almost constant at its maximum saturation level for short pulses (15 µs), significant current degradation is observed for long (100 µs) pulses. The decline occurs predominantly within the first 50 µs. However, one needs to consider that these are pulsed DC-measurements, where the transistor is in conduction state for the total length of the pulse. Less current degradation is expected during RF operation, in particular with high efficient push-pull switch mode power amplifier topologies.

The small-signal RF performance of the transistor was evaluated by calculating the maximum available gain G_{Max} from measured S-parameters. The blue line in Fig. 2

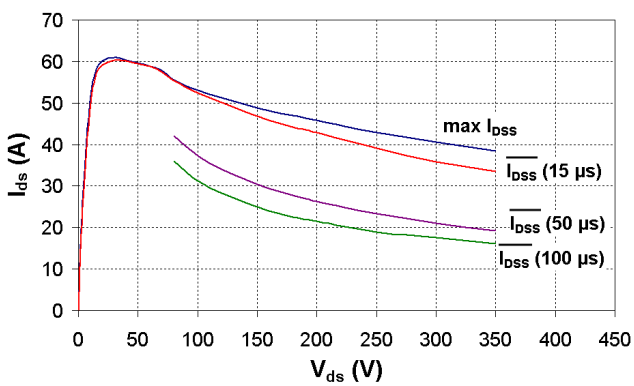

Figure 1: Degradation of pulsed drain saturation current.

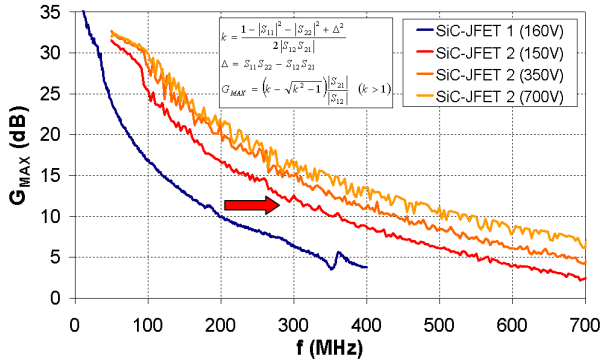

Figure 2: Small signal RF characteristic of SiC-JFETs

shows the previous transistor version (SiC-JFET1) which provided a maximum gain of 10 dB at 160 V up to ~200 MHz. The new transistor version (SiC-JFET2, red lines) shows a significant improvement in RF performance extending the usable frequency range in the 300 – 400 MHz region.

The large signal RF performance of the transistor was tested in pulsed mode in a common source class AB single ended amplifier test circuit at operation frequencies of 150 MHz and 324 MHz. The RF output power to a 50 Ω resistive load was measured at the beginning (after 10 µs) and at the end of the 100 µs long pulse. The result is shown in Fig. 3 and Fig. 4.

At 150 MHz, the new transistor (SiC-JFET2) provides at 350 V supply voltage a maximum output power of 5,6 kW at a gain of 15,8 dB. The measured drain efficiency was 74%. This is an increase in output power of almost a factor of two and an increase in gain of about 3,5 dB compared to the previous transistor version. After 100 µs, the output power is reduced to about 5 kW.

The gain versus output power at the higher frequency (324MHz) is shown in Fig.4 for the reading points at 10 µs and 100 µs. The decline in RF-output power with pulse length is here more distinctive compared to the results at the lower frequency. The drain efficiency is reduced to about 53%. The output power at the 1dB compression point is at 3,3 kW and 2,4 kW for the reading points at 10 µs and 100 µs, respectively. The maximum gain was 11,5 dB and 10,2 dB, respectively.

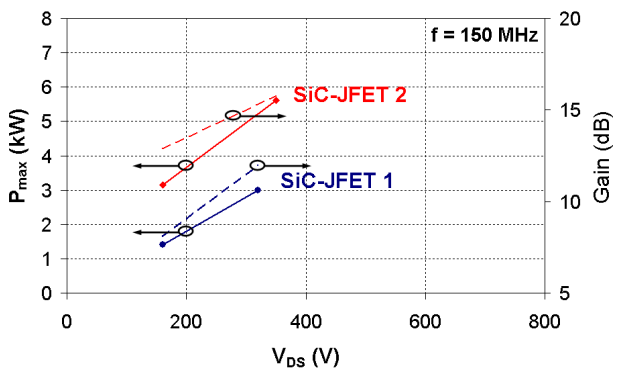

Figure 3: Large signal RF characteristic of SiC-JFETs.

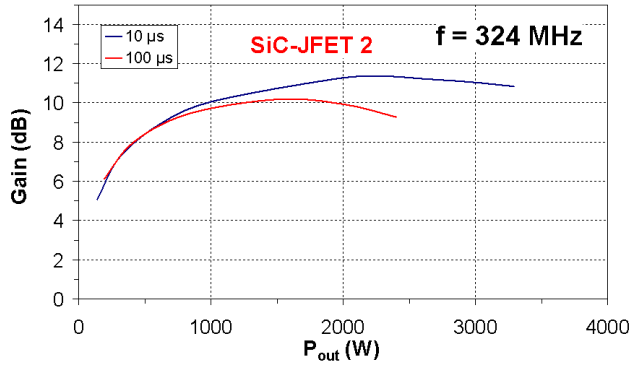

Figure 4: Gain of SiC-JFET at 350 V and 324 MHz.

SOLID STATE RF-MODULE

For the final RF-module, we used a novel planar interconnect technology (SIPLIT®, **Si**emens **Pl**anar **I**nterconnect **T**echnology, patented by Siemens 2003) to connect the transistor chips with the substrate board. The SiC transistors are directly attached to direct copper bonded (DCB) aluminium oxide ceramic substrates. In the next step, a soft, epoxy-based insulation film is applied by a vacuum lamination on the topside of the entire substrate. Vias in the insulation film are then opened by a pulsed laser to provide contact areas at the chip and substrate pads. A subsequent photo-structuring process on top of a sputtered seed layer defines the interconnect traces between the chip pads and the substrate. An electroplating Cu deposition process creates traces with a typical thickness of 50µm-200µm. In a final step the seed layer is removed by wet chemical etching. SIPLIT® enables a very compact assembly with enhanced RF- and thermal performance.

We have built very compact 75 x 90 mm ceramic RF-modules by using the previously described SIPLIT process. A picture of the RF-module is shown in Fig. 5. The modules have a fully symmetric push-pull topology (circlotron) with four transistors in parallel in each leg. The basic circuit was already described previously [1-4]. Connectors for an external capacitor bank are shown at the top and spring connectors to plug the module to the power combiner are shown at the bottom of the picture.

In combination with a suitable resonant load, the RF module can operate in class F mode at very high efficiencies. In an ideal class F operation, current and voltage are 180° out of phase and the output voltage waveform is a square wave while the drain current is a half-rectified sinusoid. A filter at the intrinsic drain of the transistor with the correct impedances at fundamental and the harmonics is required to shape the waveforms [5]. The shaping minimizes the overlap of the voltage and current waveform which reduces power dissipation in the transistor and increases the efficiency. We have started filter design based on transmission lines, but the RF-modules have been tested so far only with resistive loads. The results are presented in the next section.

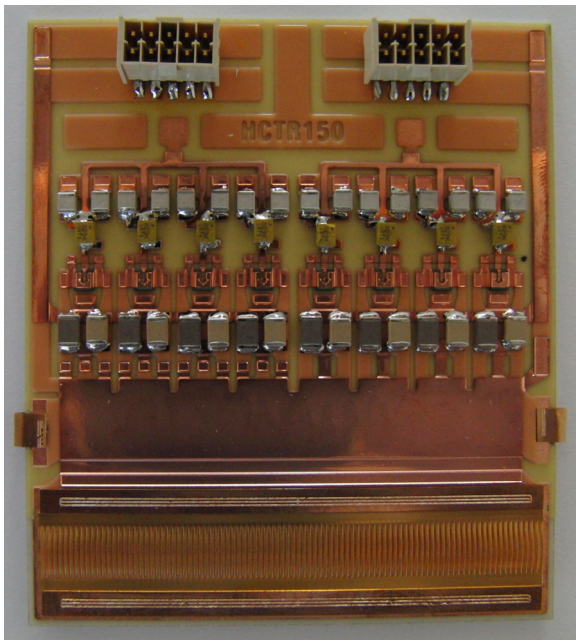

Figure 5: Solid state RF-module.

RF MODULE TEST RESULTS

The RF-modules were so far tested at 324 MHz. A Balun after the drive amplifier provides the 180° phase shifted RF-input signals for the RF-module. RF-input signals and the supply voltage are connected via λ/4 coax cables to keep the symmetry of the circlotron. An impedance matching network provides transformation between the module output and the 50 Ω load. The RF output power was measured with a spectrum analyzer after 10µs and 90 µs. The result is shown in Fig. 8.

At 350 V, the output power at the 1dB compression point was 20 kW at the 10 µs reading point and it declines to about 12,5 kW after 90 µs. If the supply voltage is increased to 450 V, the RF-module delivers up to 28 kW with a properly matched network between the output and the 50 Ω load. At the 50 µs reading point, the output power declined to about 18kW at 450 V.

The calculated module gain versus output power is shown in Fig.9. The maximum gain is in the range between 10,6 dB and 11,3 dB at 350 V and 450V, respectively.

CONCLUSIONS

Compact high power solid state RF modules based SiC transistors were developed and tested. Our second generation of RF-optimized SiC-transistors (SiC-JFET2) shows sufficient gain up to ~400 MHz. The transistors are connected to the substrate board via a novel planar interconnect technology (SIPLIT®). Depending on input power, supply voltage and pulse length, the RF-module delivers an output power of up to 28 kW at supply voltages between 350V and 450V.

The next planned steps are to implement a second amplifier stage to increase the total RF-module gain.

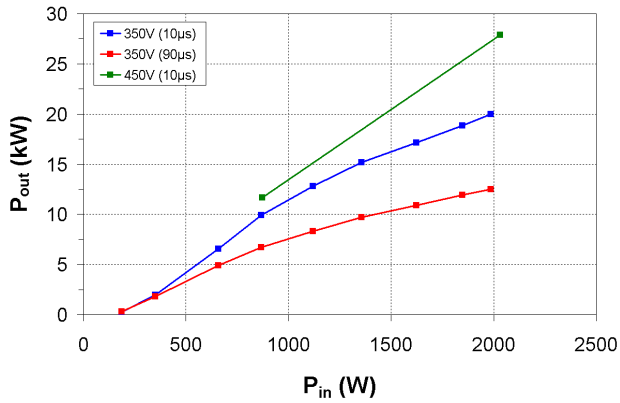

Figure 6: Output power of RF-module at 324 MHz

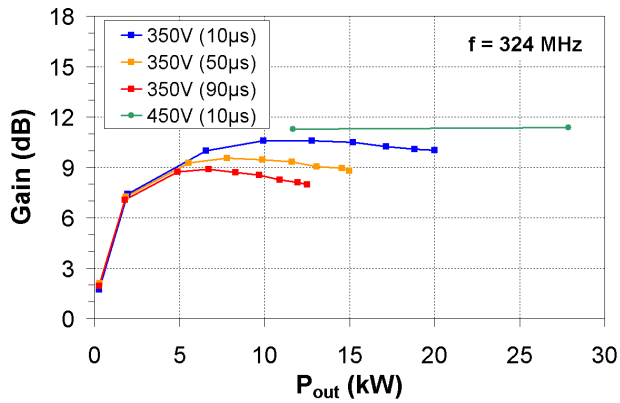

Figure 7: Large signal gain of RF-module

We are also designing a power combiner to hook-up ~100 RF modules and develop a harmonic filter to enable class F operation of the RF-module with improved efficiency.

We are confident to build RF-sources in the MW range in the near future by this modular concept based on solid state RF-modules. This could be an attractive replacement for traditional RF-sources for linear accelerators and enables new accelerator configurations like solid state direct drive® RF LINACs [3].

REFERENCES

[1] O. Heid, T. Hughes, "Solid State RF Power: The Route to 1W per Euro Cent", PAC11, New York, US

[2] R. Irsigler, R. Baumgartner, O. Heid, M. Hergt, T. Hughes, "High power SiC solid state RF-modules", PPC11, Chicago, USA

[3] O. Heid, T. Hughes, "Compact solid state direct drive RF LINAC", IPAC'10, Kyoto, Japan

[4] M. Hergt, R. Baumgartner, O. Heid, T. Hughes, R. Irsigler, "Compact 3,5 kW semiconductor RF-modules based on SiC-VJFETs for accelerator applications", IPMHVC10, Atlanta, USA

[5] F. H. Raab, "An introduction to class-F power amplifiers," RF Design, vol. 19, no. 5, pp. 79–84, May 1996.