PRESENT STATUS OF MPS AND TS FOR IFMIF/EVEDA ACCELERATOR

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Abstract

Control System for IFMIF/EVEDA accelerator prototype (IFMIF/EVEDA Acc) consists of the six subsystems; Central Control System (CCS), Local Area Network (LAN), Personnel Protection System (PPS), Machine Protection System (MPS), Timing System (TS) and Local Control System (LCS).

On the other hand, the IFMIF/EVEDA Acc provides a deuteron beam with the power more than 1 MW, which is as same as that in cases of J-PARC and SNS. Then the control system for IFMIF/EVEDA Acc is required the high reliability. In addition, the control system is also required the operability to perform the various operation for beam commissioning and etc. For the configuration of the control system to satisfy these requirements, we are developing mainly MPS and TS.

This paper presents the development status of the TS modules and EPICS (Experimental Physics and Industrial Control System) drivers for TS and MPS, and the prospects to apply them to the Injector test.

INTRODUCTION

The IFMIF/EVEDA Acc is a huge power accelerator. Then, the control system for IFMIF/EVEDA Acc must have the safety function considering the radioactivation of accelerator vault and components. And, the control and monitoring function to realize the efficient validation test is also required to minimize the radioactivation caused by the beam loss. In light of these requirements, the control system for IFMIF/EVEDA Acc is consists of six control subsystems, which are PPS and MPS for the safety function, and CCS, LAN, TS and LCS for the control and monitoring function [1].

It is important that the high reliability of hardware for control system is realized by reduction of the development risk and the initial failure. Therefore, we decided that the control system is developed by customizing proven system and hardware.

On the other hand, it is important that the interface for data communication during the control system and the accelerator subsystems is standardized, because IFMIF/EVEDA Acc is developed by some implementing agency. Then, we decided the control system is developed using EPICS.

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MACHINE PROTECTION SYSTEM

MPS realize the beam rapid stop to minimize the beam loss. The target time of MPS signal transfer, which is the time from "MPS unit received the interlock signal from accelerator subsystem" to "MPS send the beam stop signal to the injector", is less than 10 micro seconds.

On the other hand, in the case of MPS for J-PARC Linac, this is realizing "the beam rapid stop" within 5 micro seconds after MPS units received the interlock signal and "the high reliability" with few malfunction [2]. The backbone of MPS for IFMIF/EVEDA Acc will use MPS unit used at J-PARC Linac because of this performance.

Then, as the basis of this MPS unit, the interface between MPS and accelerator subsystem will be developed, and MPS will realize the logic for beam stop, beam restart and etc.

Hardware Configuration

MPS hardware configuration is shown Fig.1. Each MPS units are connected by hardwire (metal or optical cable). An interlock signal received by an MPS unit is sent to the unit for Injector at the high speed. Next, the unit for Injector sends the "beam stop signal" to Injector, and Injector will stop injecting the beam. Then, each unit is connected the PLC (Programmable Logic Controller: SIMENS S7 300) and the operator is able to control and monitor the MPS units via PLCs.

Development Status (EPICS driver)

For the remote control and monitoring using EPICS, it is necessary for development of the EPICS driver to communicate with IOC (Input/Output Controller) and

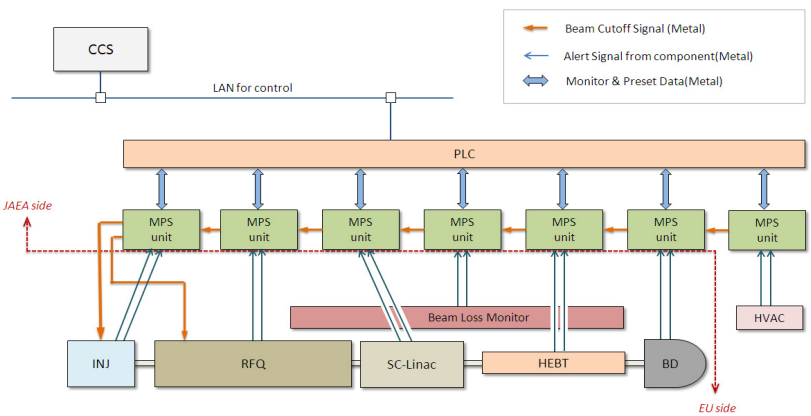

Figure 1: MPS hardware configuration.

PLC. Then, there are two ways to communicate with IOC and PLC. One is the relay communication via "OPC server" and this data path is "PLC - OPC server - IOC (in OPC server) - OPI (Operation Interface)". Another is the direct communication with IOC and PLC and this data path is "PLC - IOC - OPI". In the case of "relay communication", the data size for one communication is 32KByte. But, the data updating cycle become longer than "direct communication". On the other hand, in the case of "direct communication", the data size for on communication is 8KByte. However, the communication data size to control and monitor MPS units does not become large, because both the status signal and the control signal are bit signal. Therefore, the "direct communication" will not have major problem. Then, we developed the EPICS driver by the way of "direct communication", which is simple configuration and fast data update.

In the light of the connection with one PLC and some MPS units, in this driver, a data block on PLC is corresponded a device in EPICS record. Fig.2 shows the example of EPICS record file. In the "field(OUT, "@simatic://$(target)/DEV1P0")", the "DEV1" shows "device 1" in EPICS record, and we defined that "device 1" corresponds the "data block 101" on PLC. Then, for example, if the data blocks is defined each MPS units, it is possible to develop the EPICS record files which are easy to understand and maintain.

It is realized that one IOC connects one PLC (one MPS) (Fig. 3), and we can control and monitor the MPS using EPICS, now. Next step, we will confirm the performance of one IOC and some PLCs connection.

TIMING SYSTEM

IFMIF/EVEDA Acc is performed the CW operation. However, the pulse beam operation will be performed for aging of machine conditioning and etc. In addition, this operation will be also performed for the commissioning operation reduced the radioactivation by beam losses.

In fact, the operation will be changed from pulse to CW operation, for example, the pulse operation with short beam width is performed at first, wider the beam width and faster the beam repetition by gradation, and becoming the CW operation finally. Therefore, it is important for TS to have the performance that both pulse operation and CW operation are effectively performed. The speculated operation for IFMIF/EVEDA Acc is shown Table 1.

Table 1: Speculated Operation for IFMIF/EVEDA Acc

beam repetition	・1Hz - 0.1Hz ・Shingle shot （1 beam pulse output） ・CW
beam width (Gate width)	・a few ten micro sec. ・a few msec - a few ten msec ・a few seconds ・CW

It is more difficult for timing system to design the system for pulse operation than for CW operation. Then, the TS for IFMIF/EVEDA Acc is designed and developed, which is also performed CW operation by the customizing the system for pulse operation

On the other hand, J-PARC TS have the function to perform the pulse operation, the repetition is single beam shot, from 50Hz to about 0.1Hz, and beam width (gate

```
record(mbboDirect,
"$(mname):DEV1:PARAM1_MPS_RESET")
{
        field(DESC, "Command code")
        field(SCAN, "Passive")
        field(DTYP, "IFMIF PLC")
        field(OUT,  "@simatic://$(target)/DEV1P0")
        field(SEVR, "NO_ALARM")
}
```

Figure 2: Example of EPICS record file.

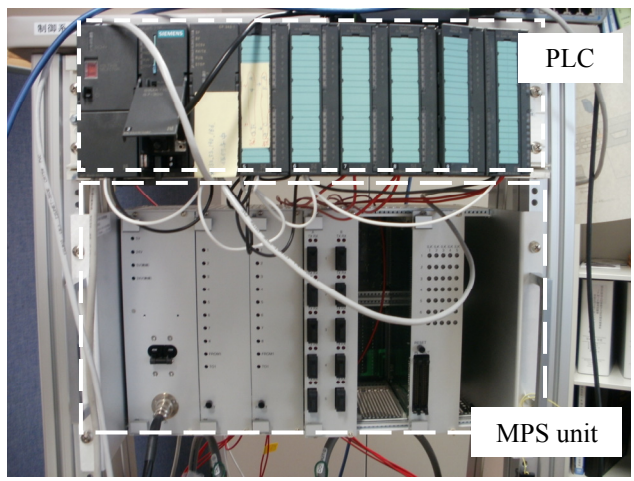

Figure 3: Connection of PLC and MPS unit.

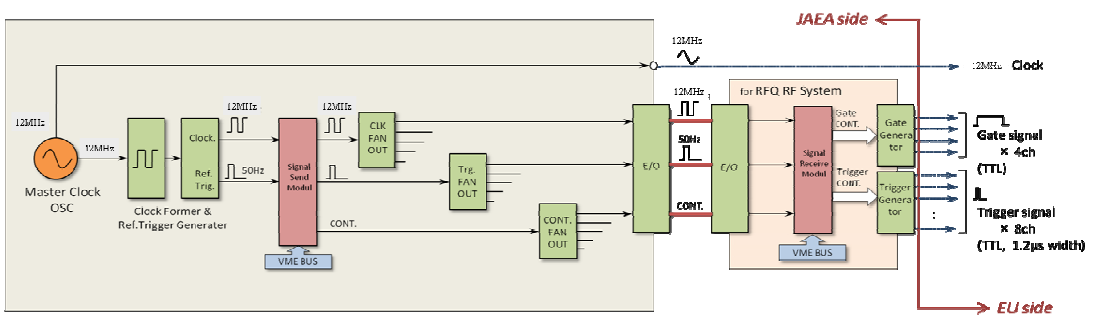

Figure 4: TS hardware configuration.

width) is from 1.2micro sec. to about 170msec [3]. Then, the beam commissioning operation to keeps to a minimum radioactivation of the components is performed by making effective use of TS function. And, this function is useful for the beam commissioning operation of IFMIF/EVEDA Acc.

Hardware Configuration

Fig.4 shows the hardware configuration of TS. TS is configured mainly the signal send module (VME), the signal receive module (VME), the trigger generator (NIM), the gate generator and etc. Send module is inputted Master Clock and Reference Trigger and makes Control Signal for TS every Reference Trigger. Then, Master Clock, Reference Trigger and Control Signal which are outputted from this module are sent the receive modules. Then, receive module receives some from a send module, and generates the delayed signals complying with Control Signal. The delayed signals are LVDS and sent to Trigger generator or Gate generator. And, "Trigger generator" and "Gate generator" generate the electrical signals complying with the delayed signals from receive module.

TS Module Customization

Then, IFMIF/EVEDA TS modules have been developed based on J-PARC TS modules. Then, IFMIF/EVEDA Acc TS receive modules have functions the gate signal is outputted whose width is about 2 sec. In particular, the counter was customized and adopted the 28bit counter (for J-PARC: 24bit). In addition, receive module also have functions the continuous gate signal is outputted by the expansion of control area for delay parameter.

On the other hand, about the TS send module, the type bank is customized and increased substantially, for J-PARC: 4 banks and for IFMIF/EVEDA: 64 banks. One type bank nearly corresponds one operation pattern. Therefore, by this customization, we can perform the efficient operation for various commissioning. In addition, it is effective that the miss operation is decreased by operating for operation pattern change.

EPICS driver for IFMIF/EVEDA TS modules are developed and we are able to control using EPICS, now. And, we perform the long run test for these modules, and these are running with no trouble (at the end of April, 2010), (Fig.5).

MPS AND TS FOR INJECTOR TEST

We are planning the test for MPS and TS in the Injector test at EU. Injector test will start in autumn 2010. Fig.6 is shown the configuration for this test. In this test, MPS part is configured one MPS unit and one PLC and this performance test has been acceptable result as noted above. In the same way, TS part test has been acceptable result. In this way, the base of hardware and software for injector test has been prepared. Then, we will implement the efficient test in injector test.

CONCLUSION

We have developed the essential part of MPS and TS for IFMIF/EVEDA. In the result, MPS is able to control and monitor from EPICS OPI using "direct communication" EPICS driver for PLC. In the same way, TS is able control from EPICS OPI and output the timing signals required from IFMIF/EVEDA Acc operation.

As the next step, we will perform the linkage test with "MPS and TS" and "Injector" in autumn, 2010. Then, results of this test will feedback "the design of interfaces between the control system and accelerator subsystem" and "the final design of MPS and TS".

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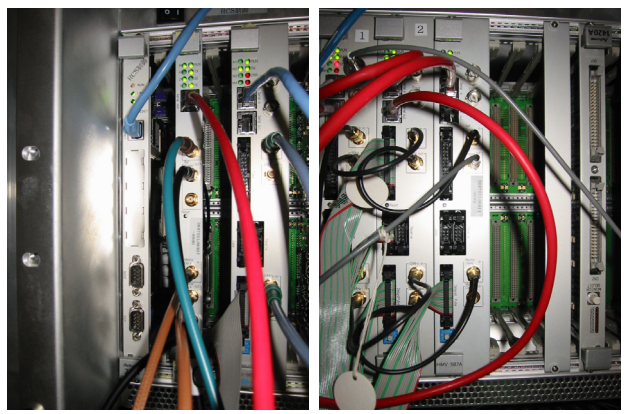

send module receive module

Figure 5: TS modules long run test.

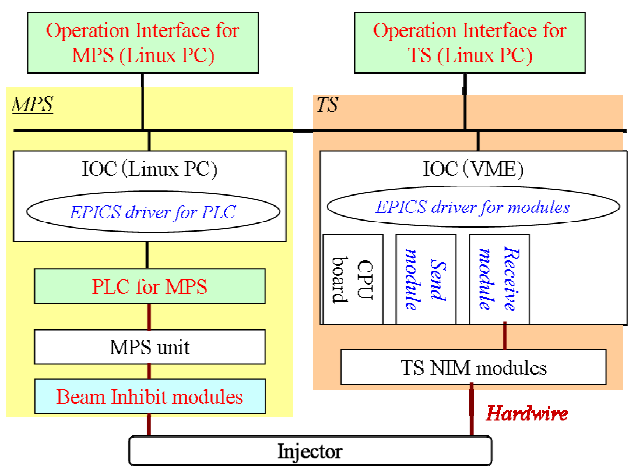

Figure 6: Configuration for Injector test.