LOW-LEVEL RF SYSTEM FOR cERL

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Abstract

The compact Energy Recovery Linac (cERL) is under construction in KEK. In order to satisfy the requirement of a high stability of the RF field, the digital low-level RF (LLRF) system has been developed on the basis of the previous experience at STF in KEK. In this paper, we describe the current status of the LLRF status for cERL.

INTRODUCTION

The 5-GeV Energy Recovery Linac (ERL) as the future light source is planned to be constructed in KEK. In order to establish the key technologies for the 5-GeV ERL, a compact ERL (cERL) is under construction. For the 5-GeV ERL, a high RF stability (0.01% in amplitude; 0.01° in phase) is required. For cERL, the stability of 0.1% in amplitude and 0.1° in phase is required. In order to satisfy these requirements, a digital low-level RF (LLRF) system has been developed on the basis of the previous experience at STF in KEK [1]. This report presents an overview of the LLRF system for cERL.

LLRF SYSTEM

The schematic representation of the LLRF system for cERL is shown in Fig.1. The components of the LLRF system are as follows:

- Digital feedback system.
- Clock generation system (1310 MHz, 40 MHz, and 10 MHz based on MO = 1300 MHz).
- Cavity tuner control system.
- Driver amplifiers for klystrons or IOTs.
- Fast interlock system (for Pf, Pr, Arc, Quench, etc.).

DIGITAL FEEDBACK SYSTEM

The digital feedback system using an FPGA is adopted in order to achieve a high stability of the cavity field. This digital signal processing technique in cERL is based on the system in STF [1]. The cavity pick-up signal of 1300 MHz is down-converted to an intermediate frequency (IF: 10 MHz). The IF is sampled by a 16-bit ADC with 40 MHz. The feedback calculation for PI control is carried out in the FPGA. The baseband signals of *I* and *Q* from DACs is fed into the IQ modulator [1].

DIGITAL CONTROL BOARD

The μTCA system is adopted for the digital control boards. These boards consist of a base card and daughter cards with ADCs or DACs. The FPGA, digital I/O, and an external trigger port are on the base card. The external trigger will be used for the burst-mode operation. A parameter setting or data acquisition is performed through the gigabit Ethernet bus at the backplane. EPICS is selected as the communication protocol. In order to install the EPICS, Virtex-5 FXT, which is an FPGA with a hard-core CPU (Power PC), is selected, and the embedded

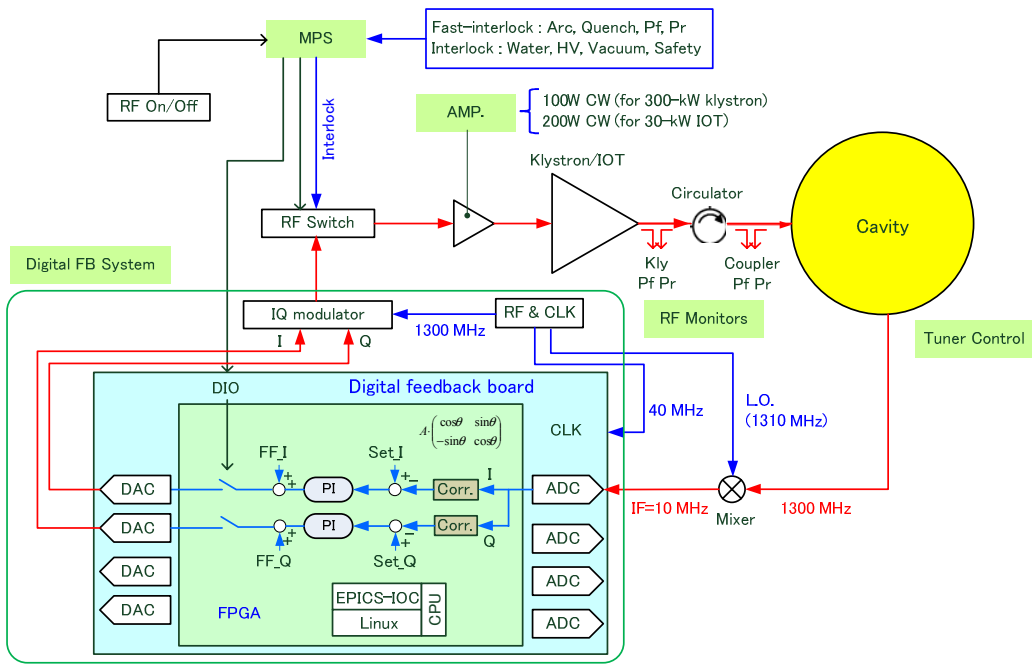

Figure 1: Schematic representation of the LLRF system for cERL.

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Linux is installed as an OS. Therefore the board becomes an EPICS-IOC [2].

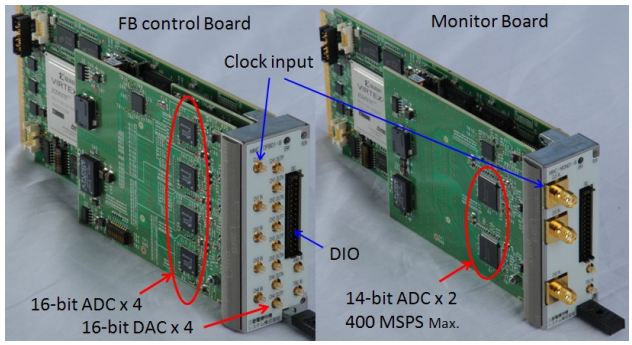

Figure 2: Digital control boards (left: feedback control board, right: monitor board).

Feedback Control Board

An ADC card and a DAC card as the daughter cards are attached on the base card. The ADC card is equipped with four 16-bit ADCs (LTC2208), a clock input, and a clock buffer and divider (LMK01010). The DAC card is equipped with four 16-bit DACs (AD9783, 2-ch/1-chip). In addition to the feedback control, quench detection is executed by the calculation of the amplitude in the FPGA.

The performance of the AD-card was tested for 10-MHz sin-wave. The isolation among input-channels was less than −80 dB. Input phase was tuned to 90° in order to measure the influence of aperture jitter. Figure 3 shows a plot of I vs Q. By comparing with the deviation of I and one of Q, the error due to the aperture jitter was not large. Figure 4 shows the result of amplitude and phase converted from I and Q data. Stabilities of amplitude and phase were 0.022% rms and 0.016° rms, respectively.

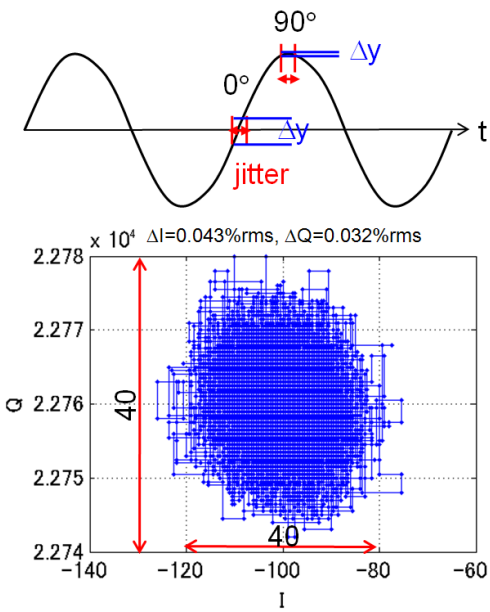

Figure 3: Plot of I vs Q at input-phase = 90°.

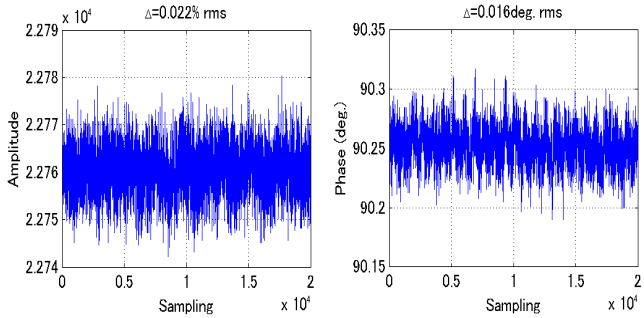

Figure 4: Result of amplitude and phase converted from I and Q data. Stabilities of amplitude and phase were 0.022 % rms and 0.016° rms, respectively.

Monitor Board

The monitor board is also manufactured. This board can monitor the 1.3-GHz signal without a down-conversion by the direct sampling method [3]. On this daughter card, two ADS5474 ADCs (14-bit, 400 MSPS, 1.4-GHz input bandwidth) are equipped with a clock input and a clock buffer and divider.

GAIN MARGIN

The field error of the cavity is compressed by a factor of the feedback gain. The stability of high-level RF components like a klystron power source [4] is designed on the basis of the feedback gain of the LLRF. In order to evaluate the amount of feedback gain, the gain margin was calculated from the Bode plot. The gain margin as a function of the feedback-loop delay is shown in Fig.5. A loaded Q (Q_L) of the main linac with an energy recovery is 2×10^7, and Q_L of the injection linac is 2×10^5 for I = 100 mA operation. For the main linac, the feedback gain can be set high as shown in Fig.5. In contrast, the gain margin for the injection linac is limited to a low value because of the low Q_L. The optimization of the feedback condition is very important for the injection linac. The

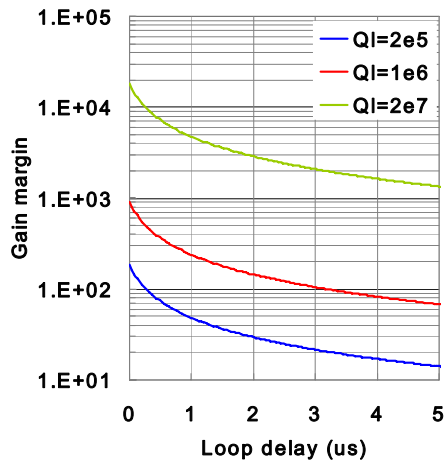

Figure 5: Plot of gain margin as a function of feedback-loop delay time.

feedback-loop delay time is required to be shorter than 1 μs at the injection linac. The LLRF station is located near the injection linac in order to minimize the loop delay.

CAVITY TUNER CONTROL SYSTEM

A mechanical tuner using a stepping motor as a slow tuner and a piezo-actuator as a fast tuner are used for correcting the cavity detuning. The same board as the digital feedback control board is employed for controlling these tuners. The phases of the cavity-input and -output signals are calculated from the *I* and *Q* information in the FPGA board. In order to minimize the generator power, feedback control is carried out for both the tuners. The pulse for the motor control is output from the digital output-port, and the signal for the piezo-actuator is output from the DAC. A protocol for the tuner control is under development.

FAST INTERLOCK SYSTEM

In order to protect the machine from the power (Pf, Pr), a discharge on the window, and a quench of the cavity, an interlock system with fast response is required. Furthermore, the interlock signal should be sent to the gun in order to immediately stop the beam injection. The fast interlock system uses the same module as J-PARC machine protection system (MPS).

MPS Module

The MPS module is shown in Fig.6. The MPS consists of ten input modules, four output modules, a CPU module, and a power module. The input module has four input channels. The output module has two input channels and two output channels. The types of input/output modules are selected from among TTL, relay, and optical boards. On the CPU module, SUZAKU [5], which is an embedded device based on a combination of FPGA and Linux, is equipped. Fast logical processing is carried out in the FPGA. EPICS is installed, and EPICS-IOC works on Linux. Therefore, the interlock status can be monitored through EPICS. Because of the flexibility of the FPGA protocol, the rightmost output module is used as an "RF ON/OFF" module with a "Local/Remote" selector.

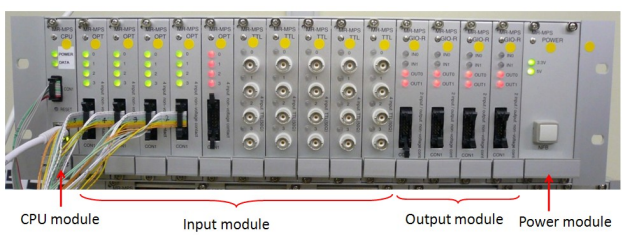

Figure 6: Photograph of MPS module.

Arc Detector

When the electrical discharge occurs at the ceramic windows of the input couplers or klystron, the RF supply should be stopped within several microseconds. Therefore, the arc detector is required to respond within 1 μs. Moreover, the error due to electrical noise should be reduced. For these purposes, the arc detector consists of an optical fiber and a photomultiplier-tube (PMT) has been developed [6]. The fiber with a large core, ϕ600 μm, is selected for obtaining a high signal-to-noise ratio. A metal material is not adopted for the jacket of the fiber cable in order to cut the ground between the arc-detector module and a noise source. Figure 7 shows a photograph of the arc-sensor module. Four PMTs (Hamamatsu H6780) are installed. The gain of each PMT is adjusted by using an LED light attached to an adapter at the head of the fiber cable.

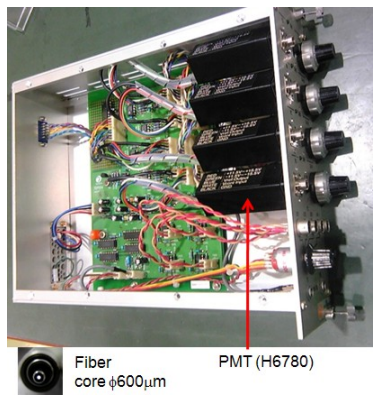

Figure 7: Photograph of arc-sensor module.

SUMMARY

The LLRF system for cERL adopted the digital feedback system for achieving a high RF stability. The new μTCA board having four 16-bit ADCs and four 16-bit DACs is manufactured for the digital feedback control. Quench detection and cavity detuning control will also be carried out by this board. EPICS is embedded in the board; the board will be EPICS-IOC. The interlock system having a fast response is also developed. The LLRF system is under development for the start of operation of cERL at the end of FY-2012.

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