A NEW TIMING SYSTEM: THE REAL-TIME SYNCHRONIZED DATA BUS

M. Liu*, C.X. Yin, L.Y. Zhao, D.K. Liu, SINAP, Shanghai, China 201800

Abstract

Currently, the real-time data transfer system is widely implemented in the accelerator control system. And the timing system is the fundamental subsystem in accelerator control system. If timing system and real-time data transfer system could be combined into one uniform system, it would be convenient to build distributed feedback system, fast interlock system and so on. So, a new timing system, the real-time synchronized data bus (RTSD bus) is developed to realize this idea. The architecture of the system and the hardware prototype design are introduced in the paper. The data exchange mechanism and system specification, including timing trigger synchronization accuracy, timing jitter relative to RF clock, data transfer rate and latency are described in detail. Redundant topology structure and fibre length compensation are specially considered. In the end, the results of testing in the laboratory and field are presented.

INTRODUCTION

In large accelerator facilities, timing information with high accuracy is needed to synchronize devices and equipments. The event timing system is a sophisticated deterministic data broadcasting system, in which signal generator broadcasts timing message to signal receivers. If signal receivers could communicate with each other, the timing function and real-time data transfer function could be satisfied in one system.

In the RTSD bus, data generated in different physical positions are transferred along with timing message in real-time. The new timing system makes the control of accelerator facilities more precisely and timely.

SYSTEM STRUCTURE

In event timing system, event generator (EVG) broadcasts timing message, and event receiver (EVR) decodes timing message to timing signal. The frame format of timing message is two bytes, one byte for event code, and the other byte for clock. The frame is automatically aligned by K character in 8b/10b coding. [1]

The fundamental structure of the RTSD bus is based on event timing system. Data is embedded in timing message so that real-time data transfer function could be realized. The frame format of timing message is changed, one byte for event code, and the other byte for data. The clock signal is generated by EVR, and is aligned by special trigger code.

In the RTSD bus, the real-time data transfer function is realized by EVR and SWITCH. EVR not only receives event code, but also exchanges data with SWITCH. SWITCH receives and decodes timing message from EVG or uplink SWITCH, and then broadcasts to downlink SWITCH or EVR. SWITCH also receives timing message from EVR, extracts data, reframes timing message with event code and broadcasts to other EVRs. The mechanism ensures not only the determinacy of timing information but also low latency of data communication.

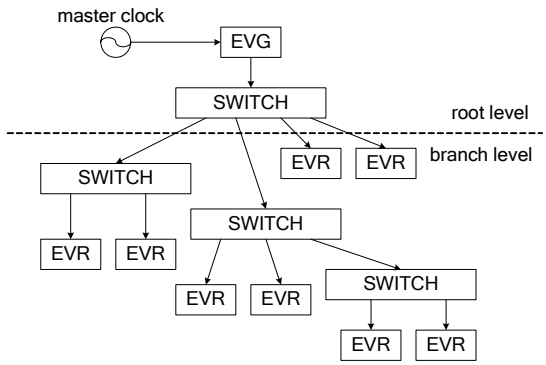

Figure 1: System structure.

Multi-level star topology is supported by the RTSD bus. The system structure of the RTSD bus is shown in Fig. 1. In the system structure, real-time data transfer function can be implemented in several private networks, but timing function is not influenced. This capability is fit for large-scale accelerator control system.

HARDWARE DESIGN

The hardware of the RTSD bus consists of EVG, EVR and SWITCH. An optical-fibre network with the rate of 2.5Gbps is utilized to build the whole structure. The preliminary prototype of modules based on VME bus has been designed, and PXI, PLC and PMC modules will be developed in future. So, the RTSD bus would be implemented in different hardware platforms.

EVG

Compared with EVG in event timing system, the hardware layout and function of EVG in the RTSD bus is the same. EVG is used to generate and broadcast timing message. The difference is that EVG sends only event code but not clocks. In the frame of timing message, one byte is for event code, and the other is blank for data exchange by EVR and SWITCH. If there is no event code to send in EVG, the synchronized frame is sent. The synchronized frame contains K28.5 character in event code field, which is used to align the frame in EVR and SWITCH.

EVG is synchronized with RF clock and AC mains voltage in order to prevent AC power interference and ensure the RTSD bus to work synchronously along with the whole accelerator facility.

* liuming@sinap.ac.cn

EVR

The layout of EVR is shown in Fig. 2.

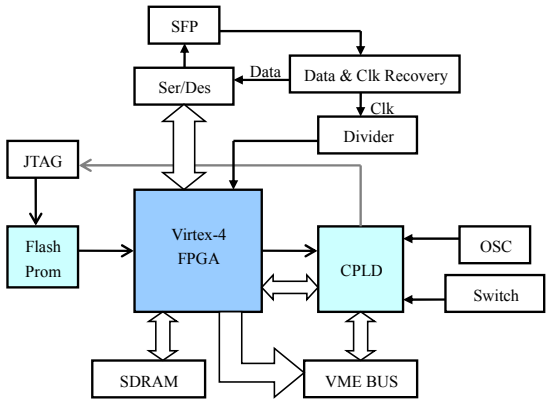

Figure 2: Layout of EVR.

EVR receives the timing message, and decodes to event code and data. The timing triggers are generated according to these event codes. Data is then further decoded and written to corresponding address of the SDRAM in EVR.

The clock signal is generated by EVR, and clock alignment is realized by a special trigger code. EVR decodes this trigger code to reset all clocks' counters. With the aid of fibre length compensation mechanism, this trigger code could be sent to all EVRs in the same time, so all EVRs output clocks could be aligned.

Once data are written to SDRAM in EVR, the data and corresponding address are encapsulated and filled into data field of timing message in sequence. By broadcasting of SWITCH, all EVRs in the same level could modify the SDRAM data in the same address space.

SWITCH

The layout of SWITCH is shown in Fig. 3.

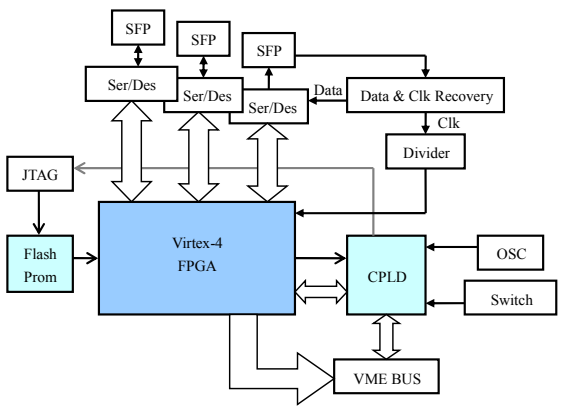

Figure 3: Layout of SWITCH.

SWITCH has two functions. One is to receive and decode event code from uplink, and then broadcast to downlink. The other function is data switching, to receive data from one downlink node and broadcast them to other downlink nodes.

The process of data switching is driven by FPGA, so the maximum latency of data transfer is fixed. The mechanism of data exchange guarantees the real-time data transfer capability of the RTSD bus, and access control between different subnets is configurable.

Hardware Specification

In the RTSD bus, the polarity, pulse width and delay of timing triggers are programmable. The baud rate in optical-fibre network is 2.5Gbps. The frequency of operation clock in EVR is 125MHz, which is 1/20 of the baud rate in fibre. Therefore, the minimum adjustable step of pulse width and delay is 8ns.

In the RTSD bus, data transfer function occupies half of fibre bandwidth. After 8b/10b coding, the maximum data transfer rate is

$$2.5\times10^{3}\times50\%\times80\%/8=125MB/s\,. \qquad (1)$$

The EVR timing signal jitter relative to the RF clock in EVG is a critical parameter in timing system. According to test results in laboratory, the RMS jitter of the RTSD bus is less than 10ps.

SPECIAL CONSIDERATION

In order to improve the performance of the RTSD bus, some special considerations will be taken into count in new version of the RTSD bus.

Redundant Topology

In order to enhance the redundancy, switched fabric should be utilized in the RTSD bus. The switched fabric uses redundant modules and channels to provide high reliability.

For example, each fibre link has two channels (SFP transceiver and Ser/Des module). When one channel is in normal mode, the other channel is in stand-by mode. If signal lost is detected by Ser/Des model, the other channel automatically switches to normal mode. The switching time is less than 1ms.

Fibre Length Compensation

In the timing system, the same type triggers are required to output simultaneously. The function of fibre length compensation in timing system could satisfy this requirement.

In the RTSD bus, SWTICH sends a query data to EVR, and measure response time of the EVR. Then SWITCH collects all EVR response time, and sets the delay step for sending timing message in each individual channel. In this way, the difference of delay time caused by fibre length could be compensated.

TEST IN LAB AND FIELD

After the completion of prototype design, the RTSD bus is tested in laboratory and field.

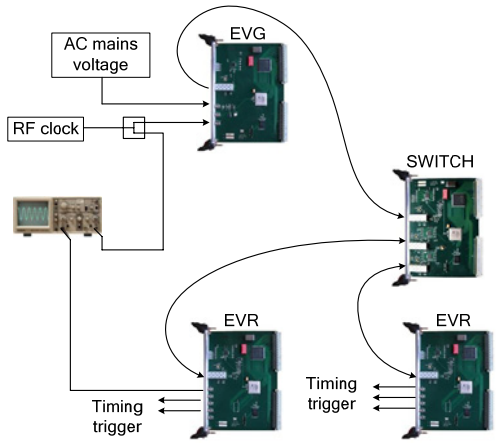

Figure 4: Layout of test bench in lab.

The layout of test bench in laboratory is shown in Fig. 4. RF clock is generated in Agilent E4400B, and then divided into 2 ways. One way is connected to EVG for synchronization, and the other way is connected to Channel 1 of the oscilloscope Tektronix TDS694C. The timing trigger from EVR is connected to Channel 2 of TDS694C.

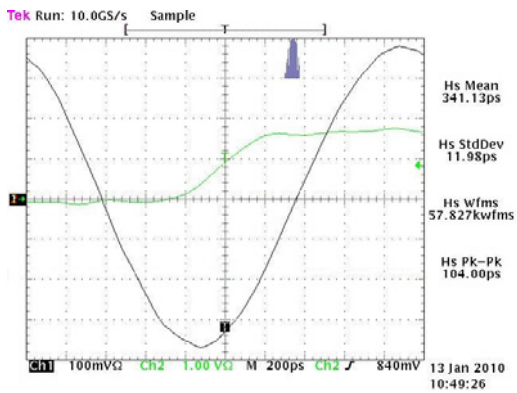

Figure 5: Jitter of timing trigger.

The test waveform in Fig.5 shows the RMS jitter of timing trigger is 11.98ps, while the oscilloscope itself contributes 6.85ps. Therefore, the RMS jitter of timing trigger relative to RF clock is 9.83ps. The excursion of mean value in Gaussian distribution is caused by temperature drift.

Then data transfer latency is measured in laboratory. One EVR sends data, and the other receives them. The delay of transmission is stabilized around 325ns.

Finally, we test EVR module in linac of Shanghai Synchrotron Radiation Facility (SSRF). According to the WCM signal of beam in Fig.6, the RTSD bus is compatible with event timing system in SSRF, and can trigger normal operation of linac.

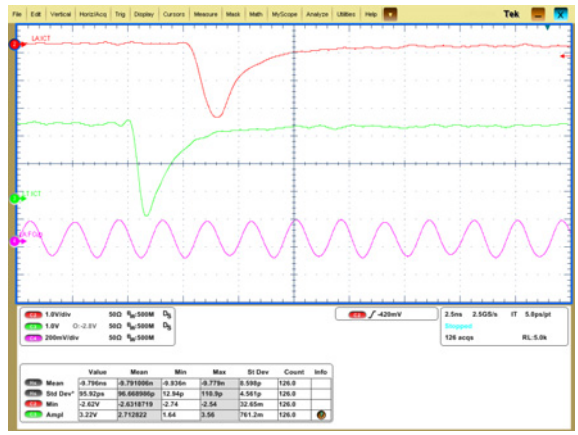

Figure 6: WCM signal of beam.

CONCLUSION

The system design and preliminary prototype of the RTSD bus have been completed. Test in laboratory and SSRF linac demonstrates that the system meets the requirement of large accelerator facilities. We will improve data transmission function, and deliver product based on PCI bus or PLC interface by the end of 2010.

REFERENCES

[1] J. Pietarinen, "Event Generator EVG-110 plus Users Manual", "Event Receiver EVR-100 Users Manual", Oct 2003, p. 6 (2003).