# THE DEVELOPMENT OF HIGH POWER SOLID-STATE AMPLIFIER IN NSRRC

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*Abstract*

A RF power source using a solid-state amplifier has become popular for accelerator applications. An amplifier array with a power divider and a power combiner yielded a power level equivalent to those using a klystron or IOT. Such a solid-state RF power source has also an advantage of easy maintenance, low cost, small DC power voltage and high flexibility. The development of a solid-state power amplifier module at 499.65 MHz using the latest RF power chip has been built to attain a power level 900 W with efficiency above 60 % of a single power module. The more power that one module can provide, the fewer modules would be required to provide the same total output power of an amplifier array. The construction of a transmitter with solid-state techniques for a RF system would thus be less complicated for easy maintenance.

## INTRODUCTION

Since year 2000, the development of a solid-state amplifier array has proved to be a reliable and attractive RF power source for accelerator applications, such as the RF amplifier commissioned for the storage ring in SOLEIL [1] at 352 MHz, 190 kW in 2006. The RF power of solid-state amplifier chips that were then available can provide up to 330 W; such an amplifier array must thus be constructed from hundreds of modules to attain a required power level. Similarly, the solid-state amplifier design for 500 MHz of 4 kW in Paul Scherrer Institute (PSI) has adopted as maximum a 280-W amplifier module as basic building block with 18 units in total [2]. So many power modules not only increase the complication of a control system, DC power distribution and RF signal combination but also occupy a great physical space. To achieve a complete RF system for an accelerator application, the increased output power of each module can effectively decrease the required total amount of modules. With the advance of the semiconductor industry for competing consumer and communication markets, more powerful solid-state amplifier chips have recently become available. Among techniques for manufacturing RF power amplifiers, a lateral diffused metal-oxide-Semiconductor (LDMOS) has shown its ruggedness and power-handling capability from ~30 MHz to 1 GHz [3].

We adopted the latest (sixth-generation), 50-V, 1200-W (at 225 MHz) LDMOS BLF578 push-pull transistor (NXP Semiconductor Co.) for initial development of a RF power module as the key and basic building block of high-power RF amplifiers array for our accelerator. With this latest 50-V transistor, a brief description of the test environment, circuit design, bias conditions of two types and pulse-output power related to gain, efficiency and power dissipation have been done at 499.65 MHz, the frequency of TLS and TPS. These experimental results assist us to specify the required number of modules, water-cooling capacity, power rating of RF connection components, control method and electrical power for a new RF power-station design. The test environment for this LDMOS transistor is shown in Figure 1.

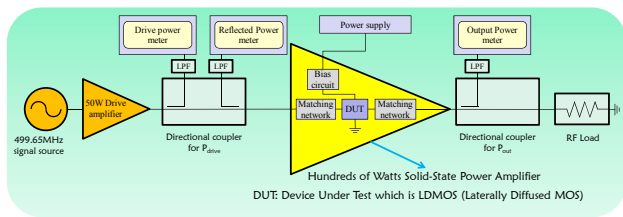


Figure 1: Test setup for sixth-generation 50-V LDMOS chip.

## CIRCUIT TOPOLOGY OF THE RF AMPLIFIER

To implement the LDMOS as a RF power amplifier, the chips are soldered on printed circuit boards using a traditional circuit schematic for push-pull topology as shown in Figure 2. This topology is popular to implement a push-pull amplifier from HF to UHF.

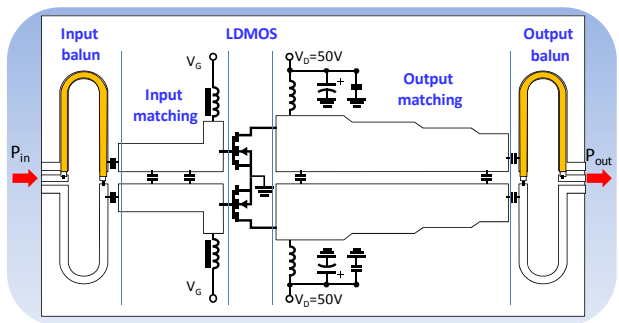


Figure 2: The schematic of power amplifier test board.

The schematic is divisible into five sections: from left to right, input balun, input matching, RF power LDMOS, output matching and output balun. The balun works as a power divider and makes the divided signal out of phase for the pair of transistors. Before the driving power enters the transistors, the input matching network transforms the 25-Ω impedance at the balun output to the input impedance of the power MOS. After that, two transistors identical inside the chip are carefully greased with a thermal compound between a flange and a heat sink and then bolted down with screws to an appropriate torque. This step is important for proper dissipation of thermal

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power to a heat sink; otherwise, the chip would overheat to fail in a short time. The output-matching network is then transforms the output impedance of the transistors to 25 Ω to be converted to a single-ended output with an output balun. In general, the input/output impedance of the transistor at such a power level would be in the range of 1-3 Ω, which is small. A sufficiently long microstrip line between the balun and the chip can aid to realize the proper impedance on tuning the position and value of capacitors during the power optimization.

## TEST ENVIRONMENT

After the fabrication of the solid-state amplifier, the circuit would then be mounted on a test stand to optimize the performance and for measurement. The principle of the test stand is basically the extent of Figure 1 with the addition of a machine to pump cooling water and a hot S-parameter measurement setup for initial matching tuning of the output. A block diagram for water cooling is shown in Figure 3; the cooling water flows through the bottom case of the amplifier. So far, the capacity of our present water cooler can absorb the maximum thermal power generated by a chip of 250 W with the chip case at 70 °C.

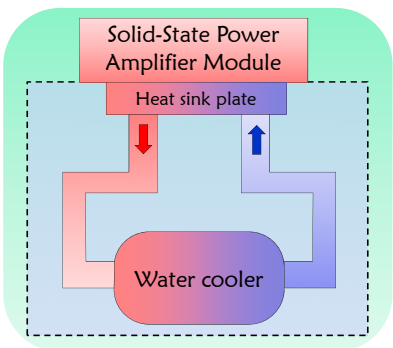


Figure 3: The water cooling concept.

Besides, to realize matching of the output impedance in the least time, the hot S-parameter is implemented [4] as shown in Figure 4. With the proper choice of coupling coefficient of the coupler, frequency of the probe tone (200 kHz from the main tone) and power level of the probe tone (1 W), the first output impedance can be realized without much difference to a large signal S-parameter.

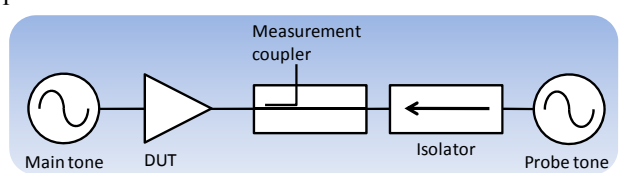


Figure 4: The Hot S-parameter for S22.

## MEASUREMENT RESULTS

After the most tedious step of impedance-matching tuning, the performance of the designed amplifier using the specified LDMOS FET can be tested. Two amplifiers operated at two bias conditions: slight class-A (simply called class-A) and deep class-AB (simply called class-AB) amplifiers are designed for a comparison. For class-A operation, the transistor is biased at drain current 1.5 A, whereas in class-AB operation the transistor is biased at a drain current 80 mA. The input and output impedance-matching networks of both circuits are fine-tuned at their bias condition. As the output power, gain and power-added efficiency (PAE) are sensitive to both impedance and impedance-tuning, the skill depends much on the experience of the RF engineer; boards have varied characteristics, but the results still can be used to indicate the trend of future system design. Incidentally, the gate-source threshold voltage of a LDMOS transistor is inversely proportional to temperature; the drain current would decrease significantly as the temperature of chip increases while the RF is on. To obtain a performance at the same ambient temperature, the graphs shown here are recorded while the case temperature of the chip is less than 30 °C. For continuous-wave (CW) operation, if the cooling system is unable to absorb the total heat generated by the chip, the heat would gradually accumulate on the chip until chip failure at extremely high temperature.

The test results are shown below. First, the output power at 499.65 MHz is plotted as a function of input drive power/W in Figure 5. This test is terminated at drive power 20 W; the maximum output power of class-A amplifier is hence ended about 800 W, but a class-AB amplifier can generate up to 900 W at the same drive input power. Impedance matching strongly affects this result; theoretically, the class-A amplifier should have larger power gain than that of class-AB. Further fine tuning is necessary if excellent class-A operation is required at greater output power.

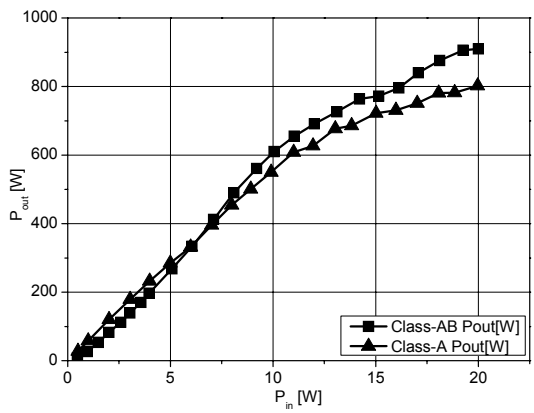


Figure 5: Output RF power vs input drive RF power

Graphs as a function of RF output power to load ($P_{out}$) follow. In Figure 6, the power gain (gain) defined as output RF power divided by input RF drive power is plotted as a function of output RF power. A class-A amplifier has greater power gain than a class-AB amplifier at smaller output power. When the output power is near saturation, the power gain of both amplifiers differs less than 1 dB.

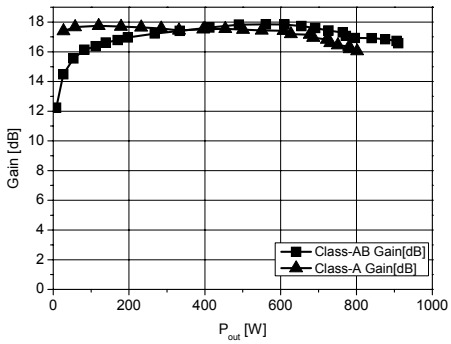


Figure 6: Amplifier power gain vs output RF power to a load.

The power-added efficiency (PAE), defined as the output RF power minus input drive RF power then divided by DC input power, is plotted as a function of output RF power in Figure 7. The class-AB amplifier has PAE greater than 60 %, much greater than for a class-A amplifier. This result agrees satisfactorily with the theory.

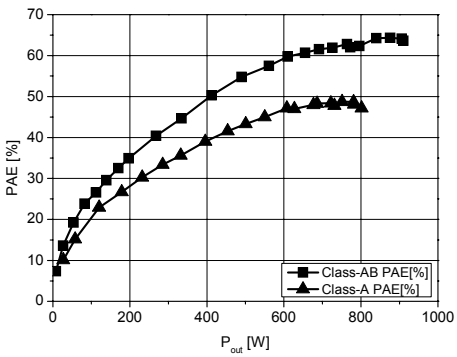


Figure 7: Power-added efficiency as a function of output RF power to load.

To estimate a future design of a cooling system, the dissipated heat power is then plotted as a kind of index. The dissipated heat power ($P_{diss}$), defined as DC input power minus output RF power excluding the input drive RF power, is plotted as a function of output RF power in Figure 8. The class-A amplifier shows greater dissipation of heat power than a class-AB amplifier by 400 W. It requires cooling capability 900 W for output RF power 800 W of a class-A bias. A class-AB amplifier would, however, require cooling capability only about 500 W at output power 900 W for CW operation.

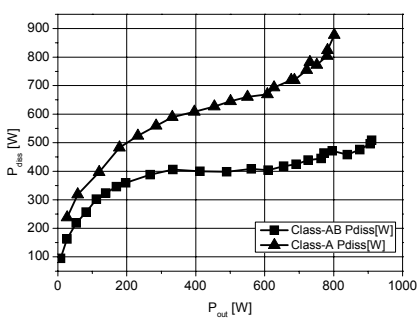


Figure 8: The dissipated heat power as a function of the output RF power to load.

## DISCUSSION

The RF amplifier for accelerator application requires CW operation. The state-of-the-art solid state chip technique providing the power level of about 1 kW is designed to operate at pulse mode without introducing much burden on cooling system. At present, the cooling speed of cooling system in house of NSRRC has not achieved the requirement of the CW operation of the amplifier module presented in this study. More effort is needed to achieve higher cooling capability especially for the small surface area-3cm$^2$ of chip flange as well as CW operation.

## CONCLUSION

We have implemented a solid-state amplifier module using a sixth-generation LDMOS for UHF band up to 900 W at 499.65 MHz in a class-AB bias with power gain about 16.5 dB and PAE greater than 60 % for a case temperature less than 30 $^{o}$C. Another amplifier using the same chip biased in a slight class-A region is applied for comparison. This work has proved the potential of the specified LDMOS chip to have output power per module to have much more power than that used in present accelerators; adopting the novel semiconductor techniques would yield a RF station of a more compact design.

## ACKNOWLEGEMENTS

We thank Mr. Sun Yi in IHEP Beijing for valuable comment and information about solid-state techniques. The technical support of Fu-tsai Jung and Ming-Hsun Tsai in NSRRC is also greatly appreciated.

## REFERENCES

[1] P. Marchand, etc., "High Power 352 MHz Solid State Amplifier Developed at the Synchrotron SOLEIL," Physical Review Special Topics – accelerators and beams, Vol. 10, p. 112001-1 (2007).

[2] M. Gaspar and M. Pedrozzi, "500 MHZ Solid State Amplifier Design Results of the 4KW Prototype," ESLS–RF Meeting, Oxford, UK (2008), http://www.cells.es/ESLS-RF/2008.

[3] M. Di Giacomo, "Solid State RF Amplifiers for Accelerator Application," PAC09, Vancouver, Canada (2009).

[4] J. Martens and P. Kapetanic "Probe-Tone S-Parameter Measurements," IEEE Transactions on MTT, Vol. 50, No. 9, p. 2076 (2002).