INDUCTION ACCELERATION SYSTEM FOR KEK DIGITAL ACCELERATOR *

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Abstract

The KEK PS-Booster which had finished thirty years of operation in 2006 is currently under renovation as a digital accelerator (DA) [1]. The first plan of us is to accelrate an argon ion beam using the induction accleration system which was developed at KEK [2]. The acceleration devices is described and the acceleration scenario in a case of Ar^{8+} is given in details. For the induction acceleration, beam bunch monitors and front-end processors is crucial devices to pick up information of the circulating beam timing with accuracy. R&D works of those components are discussed.

INTRODUCTION

A novel concept of synchrotron called *induction synchrotron* (IS) was developed at KEK in 2006 [2]. In the IS, charged particles are accelerated by pulse voltages generated through 1:1 transformers, that is called induction cells (IC), driven by switching modulators employing high power semiconductor switching elements (MOSFET). MOSFETs are turned on and off by gate signals which is digitally manipulated from the circulating signal of an ion beam. Consequently, the acceleration is always synchronized with the revolution of ion beam irrespective of the mass and charge state of ion. Thus, an IS is free from the limitation of bandwidth, unlike in RF cavities or amplifiers. Hence this feature allows us to accelerate ions in an extremely low velocity region. Acceleration of very slow heavy ions, such as cluster ions is possible [3]. The IS is called the *digital accelerator* because it does not use sinusoidal waves but pulse voltages triggered by digitised beam bunch signals.

ACCELERATOR DEVICES

The acceleration system consists of the DC power supplies (DCPS) with an output voltage of 2.5kV, the switching power supplies (SPS) that has the ablity of 1 MHz pulse modulation at maximum, and the induction cells (IC). Figure 1 shows a picture of ICs in the DA-ring.

We have two types of ICs; one is a 1 to 1 transformer (Type-1) in which the maximum pulse length is 0.5 μs; another one is a 1 to 2 transformer (Type-2) capable of generating 2-μs-long pulses with an expense of reduction in the output voltage.

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In the first stage of the KEK-DA, the acceleration of argon ions is assumed. Ar^{8+} generated in the ECR ion source embedded in the 200 kV high-voltage terminal are injected into the DA ring through the low-energy beam transport line placed downstream from the momentum separator. The power supply for the bending magnets has been already modified to allow the 10 Hz operation.[1]

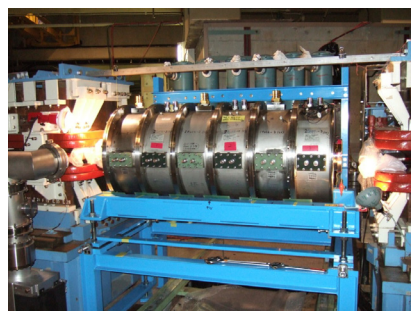

Figure 1: Induction cells installed in KEK-DA ring.

Long-term Stability of the Acceleration Devices

To test the long-term stability of the induction acceleration system, one week (from Monday morning to Friday evening) heat run without beam was performed. As explained below, we need four ICs for acceleration and two ICs for confinement; in total six ICs were continuously triggerd with 1 MHz switching frequency during a week *i.e.* for over 100 hours without big troubles.

ACCELERATION SCENARIO

The revolution period (T_r) and the required accelerating voltage of KEK-DA are calculated from the sinusoidal ramping pattern of the bending magnets. Assuming Ar^{8+}, T_r changes from 13.6 μs to 0.753μs with acceleration. The maximum accelerating voltage of 3 kV is required at the middle of the acceleration cycle.

The acceleration devices, which had been developed for the induction synchrotron experiment at KEK-PS, have crucial limitations. The output voltage of the DCPS is finite (the maximum value is 2 kV) and cannot be varied during the acceleration cycle, and the maximum switching frequency of the SPS is 1 MHz. Now two sorts of IC are available as stated in previous section. It is described below how the acceleration scheme in the KEK-DA is realized by systematically combining Type-1 and Type-2 ICs with the operational limitations of fixed output voltage and limited pulse length [4].

The acceleration cycle is divided into three stages. Figure 2-1~3 shows a conceptual diagram of the scenario from the stage 1 to 3. In the 1st stage (2 μs < T_r < 13.6 μs), a long accelerating voltage is required as mentioned earlier. Two Type-1 ICs are triggered in series to produce a long voltage pulse. Furthermore, the trigger pulse density of these ICs is controlled so that an integrated accelerating voltage for a short time period is equal to the required accelerating voltage. In the 2nd stage (1 μs < T_r < 2 μs), a set of Type-1 and 2 are simultaneously triggered because a higher effective acceleration voltage is required. In the 3rd (0.753 μs < T_r < 1 μs), two pairs of the combination of Type-1 and 2 are intermittently operated.

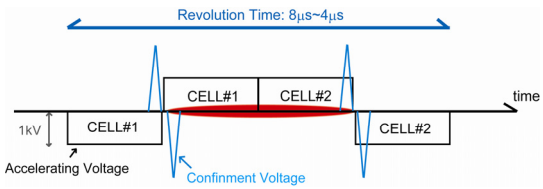

Figure 2-1: 1st stage of acceleration (2 μs < T_r < 13.6 μs). To generate a long accelerating voltage, two Type-1 ICs are triggered in series.

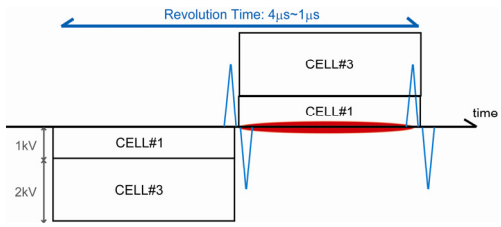

Figure 2-2: In the 2nd stage (1 μs < T_r < 2 μs), a set of Type-1 and 2 ICs are simultaneously triggered.

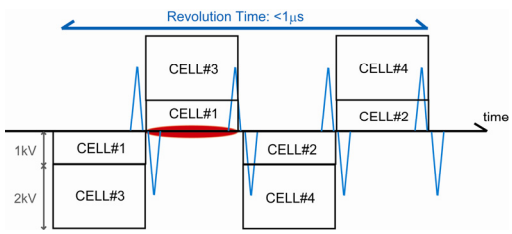

Figure 2-3: In the 3rd stage (0.753 μs < T_r < 1 μs), two pairs of the combination of Type-1 and 2 ICs are intermittently operated.

Beam Simulation of Longitudinal Motion

Beam simulation for the KEK-DA for Ar^{8+} was carried out using a particle tracking code [5]. The code calculates particle motions in the phase space assuming the DA parameters (ramping magnetic field, acceleration/confinement voltages, momentum aperture, and so on.). The longitudinal phase space plots are shown in Figure 3-1 and 2, at injection and near extraction. Confinement voltage pulses shown in lines are narrow pulses of 200 nsec width with opposite polarity. A width and height of the acceleration voltage pulse vary as a function of revolution time, as described in the acceleration scenario.

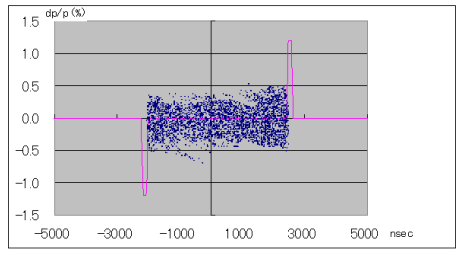

Figure 3-1: Phase plot of Ar^{8+} beam after injection (after 100 turn). Dots show injected ion particles and lines are corresponds to confine voltages (unit:kV).

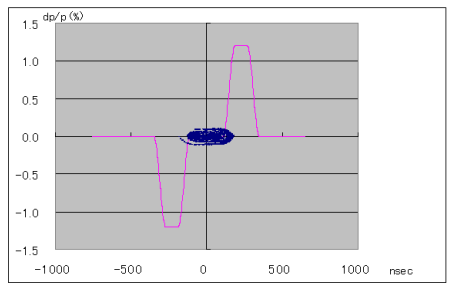

Figure 3-2: Phase plot of Ar^{8+} beam just before extraction (50ms).

GATE TRIGGER SYSTEM

The pulse length of accelerating voltages must be gradually changed with acceleration. In addition, at the stage 3 the intermittent operation of the induction acceleration system is required because the revolution frequency exceeds 1 MHz. These requirements are achieved by controlling the gate trigger signal for the solid-state switching elements. Another requirement of the gate control comes from a fact that accelerating voltages must be triggered with a variable delay from the bunch signal timing, because the flight time of an ion bunch between the bunch monitor and ICs, which are separately placed along the accelerator ring, varies with acceleration [6].

An intelligent gate control system to fulfill these requirements has been proposed. It consists of digital signal processors (DSPs) and logic circuits, which process beam bunch signals and produce trigger signals for SPSs.

DSPs

As the core of the intelligent trigger system, DSPs manufactured by Texas Instruments Co. Ltd are employed. The DSP (DSK6416T) can be programmed using the C-

language; it has 32-bit timers with a clock frequency of 128 MHz. The program obtains timing information from the ramping pattern of the bending magnets and calculates the necessary delay time, then generate the trigger pulse.

To change the pulse width of accelerating voltages with acceleration, four DSPs for one cell are required; for the timing of the start/stop signals of each set/reset pulse voltage. By varying the distance between the start and stop pulse, the pulse width can be controlled.

Stage Selector

The intelligent trigger system must know its present stage in order to vary the combination of accelerating voltages and to start the intermittent operation. Another counter is used to monitor the time in operation and inform it to the entire system. By using two DSPs, a level signal generator is established. It is called the *stage selector* and has four outputs to trigger a signal divider.

Signal Divider

As mentioned in earlier, the revolution frequency is greater than 1 MHz in stage 3, and exceeds the limitation of the switching devices, MOSFETs. To avoid a breakdown of the MOSFETs in excessive of heat deposit, the trigger signal is divided for 2 sets of ICs. We develop a module called the *signal divider*: A combination of frequency divider and multistage OR modules. The signal divider generates the trigger signal during stages 1 and 2. In stage 3, the signal divider blocks every two signals for two sets of cells; in other words, the signal divider triggers two sets of ICs, alternatively.

BEAM MONITORS

The intelligent gate control system of KEK-DA triggers the acceleration cells based on the timing signal of circulating beam bunch. A non-destructive beam monitor to obtain the timing signal every turn is requested.

One of the candidates is a current transformer (CT). We are planning to utilize the magnetic core of our induction cell itself as a CT. A voltage induced by the beam current on the primary loop should reflect the beam pulse information. The magnetic material is Finemet® which has large relative magnetic permeability. We have examined the property of the CT. In the 1-turn setup, the sensitivity (voltage/current) is about 300, but the large droop. We are developing a droop compensation circuit that amplify a signal in a low frequency region to monitor the beam bunch profile with high fidelity.

FRONT-END PROCESSING

From the injection to the extraction in KEK-DA, an ion beam bunch changes its bunch length from 4 μs to 400ns. As a result, the pulse height of beam bunch signal grows for 100 times. This feture makes it difficult to set one threshold value to get beam timing in the noisy environment of accelerator ring (Figure 4). Another problem to be expected is double-counting of the beam timing when the beam shape has double-peak or more. We are studying two strategy described below.

Waveform Capturing of Beam Bunch by ADC

Recent developments of ADCs (analog digital converters) enable us to capture the analog signal in high resolution and in high speed. The extent of the bunch signal height variation is about 100 times in voltage and the revolution frequency reaches to more than 1 MHz. Requested resolution of the ADC is more than 12-bit, considering noise effects in the readout circuit. A high speed 12-bit ADC which has the sampling rate more than 100MS/s is commercially available. We are planning to prepare a front-end board which mounts the ADC, capture the beam bunch shape and process with the DSP to identify the precise bunch center.

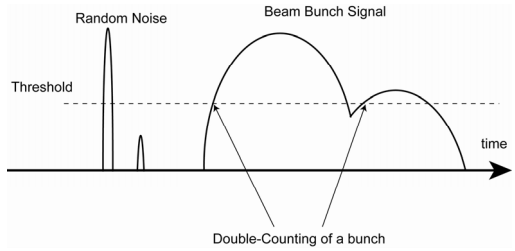

Figure 4: Difficulty in picking up the information of beam bunch timing by setting a simple threshold.

SUMMARY

The KEK-DA, the first all-ion induction synchrotron is under construction. The acceleration devices are installed in the DA ring and long-term heat run for 100 hours was performed. Gate trigger system using DSPs are ready, beam bunch monitors and front-end processors are under study. Commissioning of KEK-DA with Ar^{8+} beam is planned to be within FY2010.

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