The PLL Algorithms of the Function Generator/Controller

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ICALEPCS'15

Contents

- ✓ **Overview**
- ✓ **Synchronization and Regulation**
- ✓ **FGC Phase-Locked Loops**

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- **Synchronization and Regulation**
- **FGC Phase-Locked Loops**

Function Generation Controller version 2 (FGC2):

- Designed between 2000 and 2003
- ~1700
- @LHC

Function Generation Controller version 3 (FGC3):

- Designed between 2007 and 2011
- ~300
- @Linac4, Booster, ISOLDE, AD, LHC Inj. Upgrade,…

Linac4

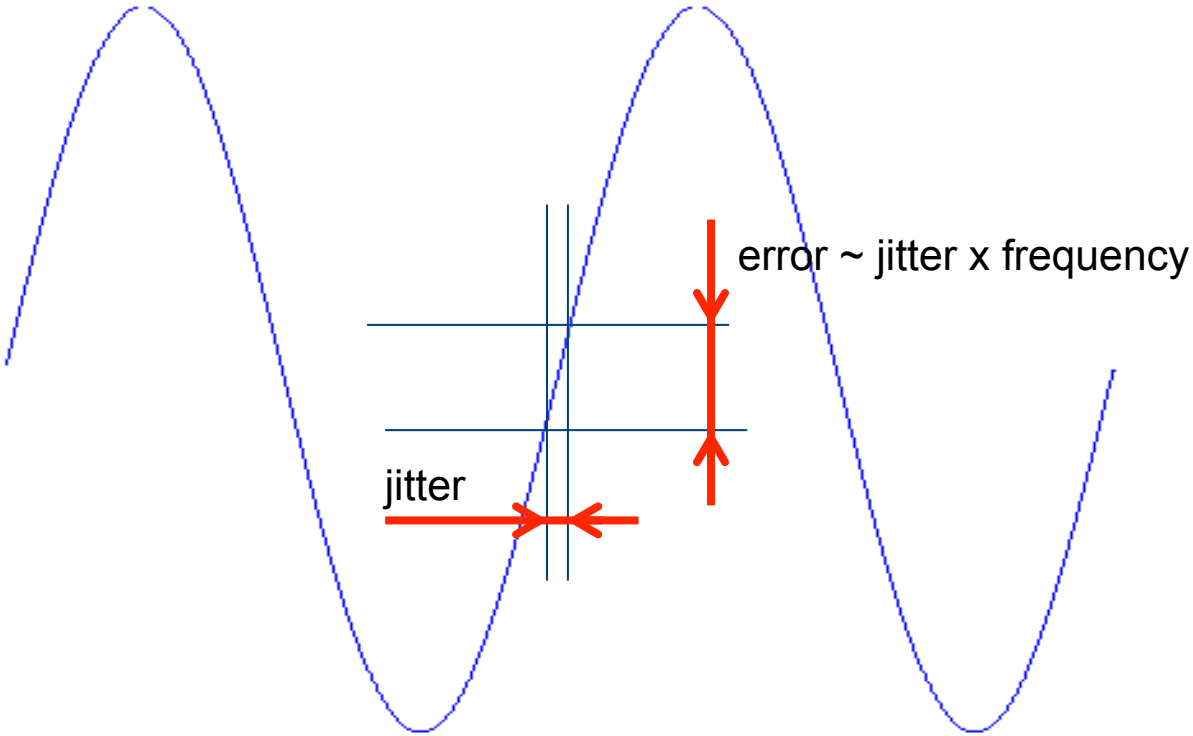
Proton Synchroton Booster

- Overview
- ✓ Synchronization and Regulation
- FGC Phase-Locked Loops

Synchronization and Regulation

Synchronization and regulation are related:

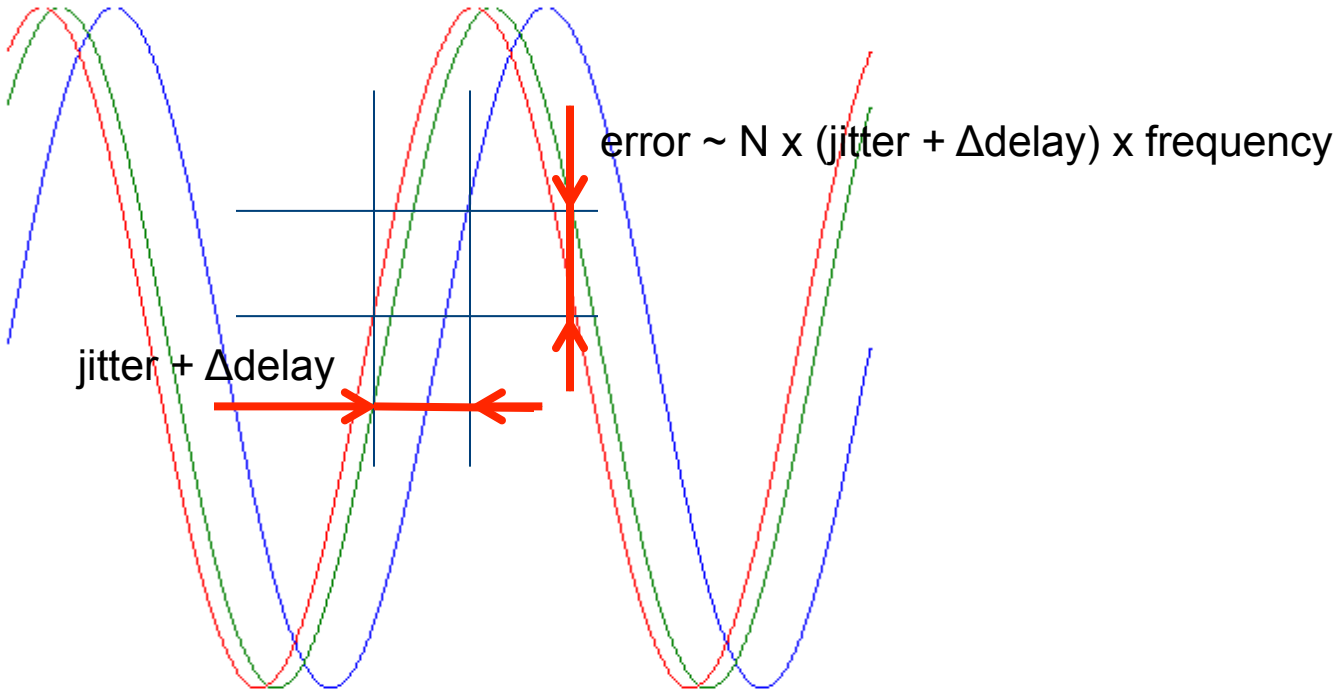
- Unsynchronized sampling ➔ Δerror



Synchronization and Regulation

Synchronization and regulation are related:

- Unsynchronized sampling ➔ jitter ➔ Δerror
- Several subsystems ➔ jitter + delays ➔ Δerror



Synchronization and Regulation

Synchronization and regulation are related:

- Unsynchronized sampling ➔ jitter ➔ Δerror
- Several subsystems ➔ jitter + delays ➔ Δerror
- Jitter and delay ➔ ∇stability

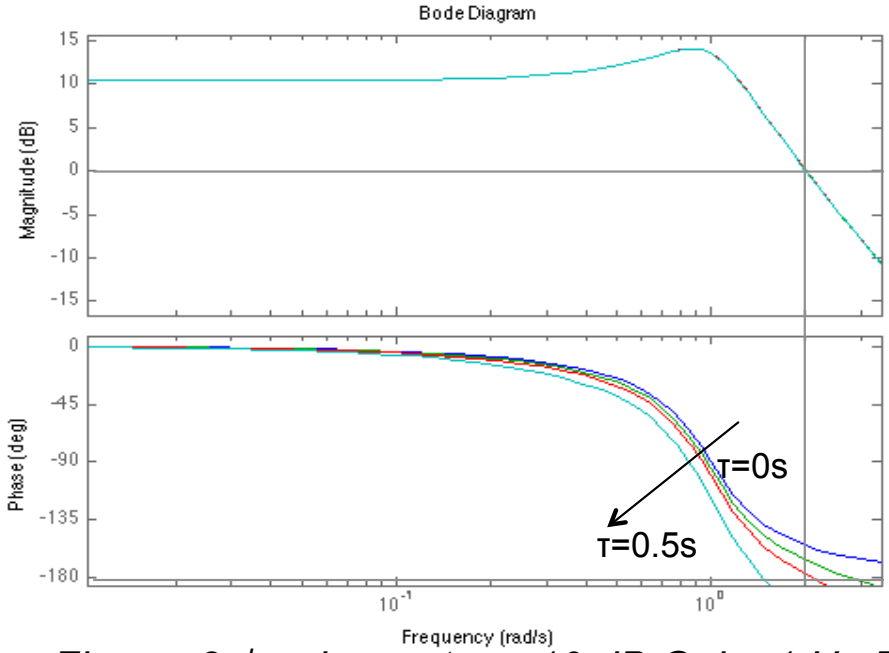
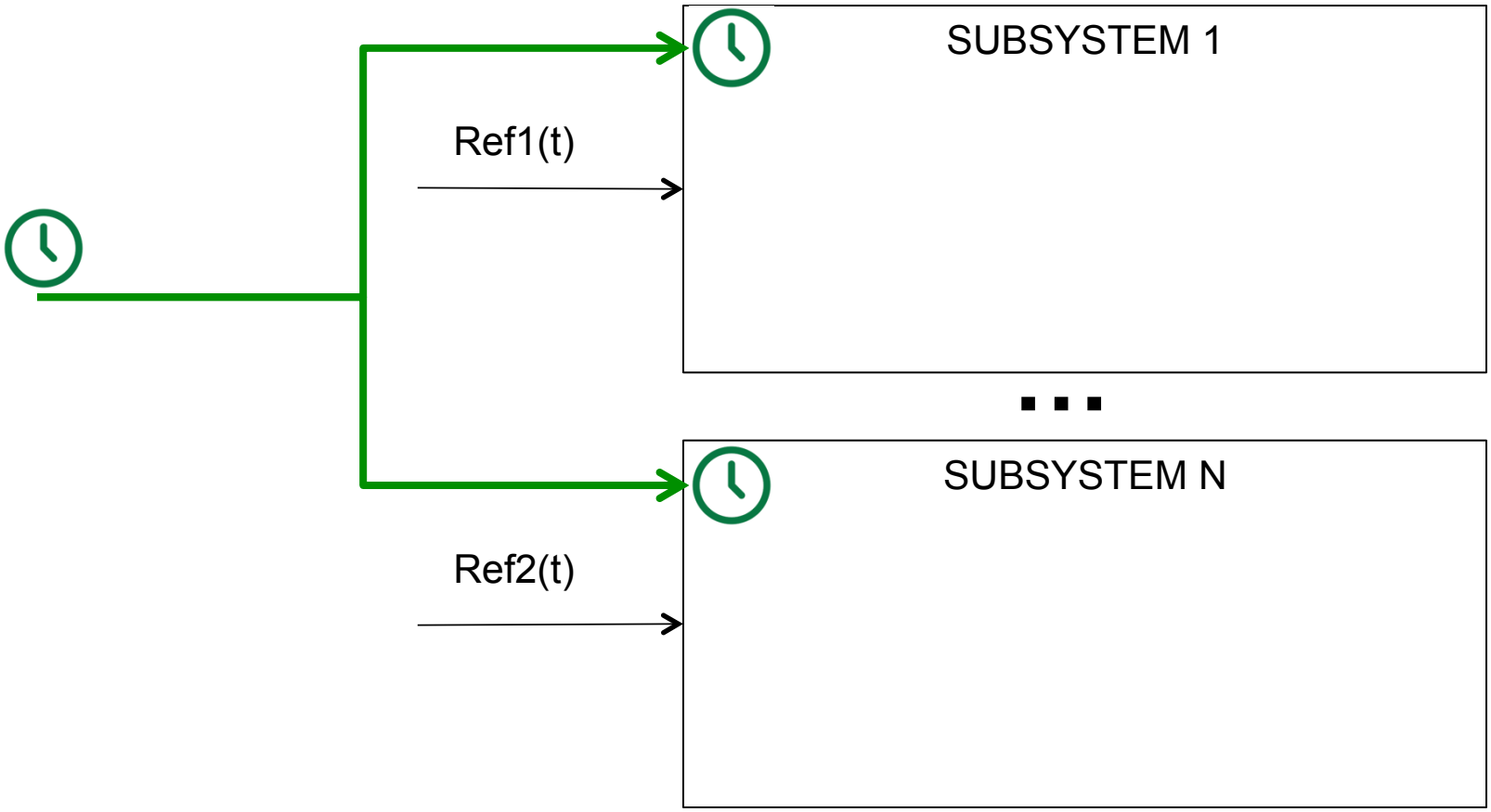


Figure. 2nd order system, 10 dB Gain, 1 Hz BW

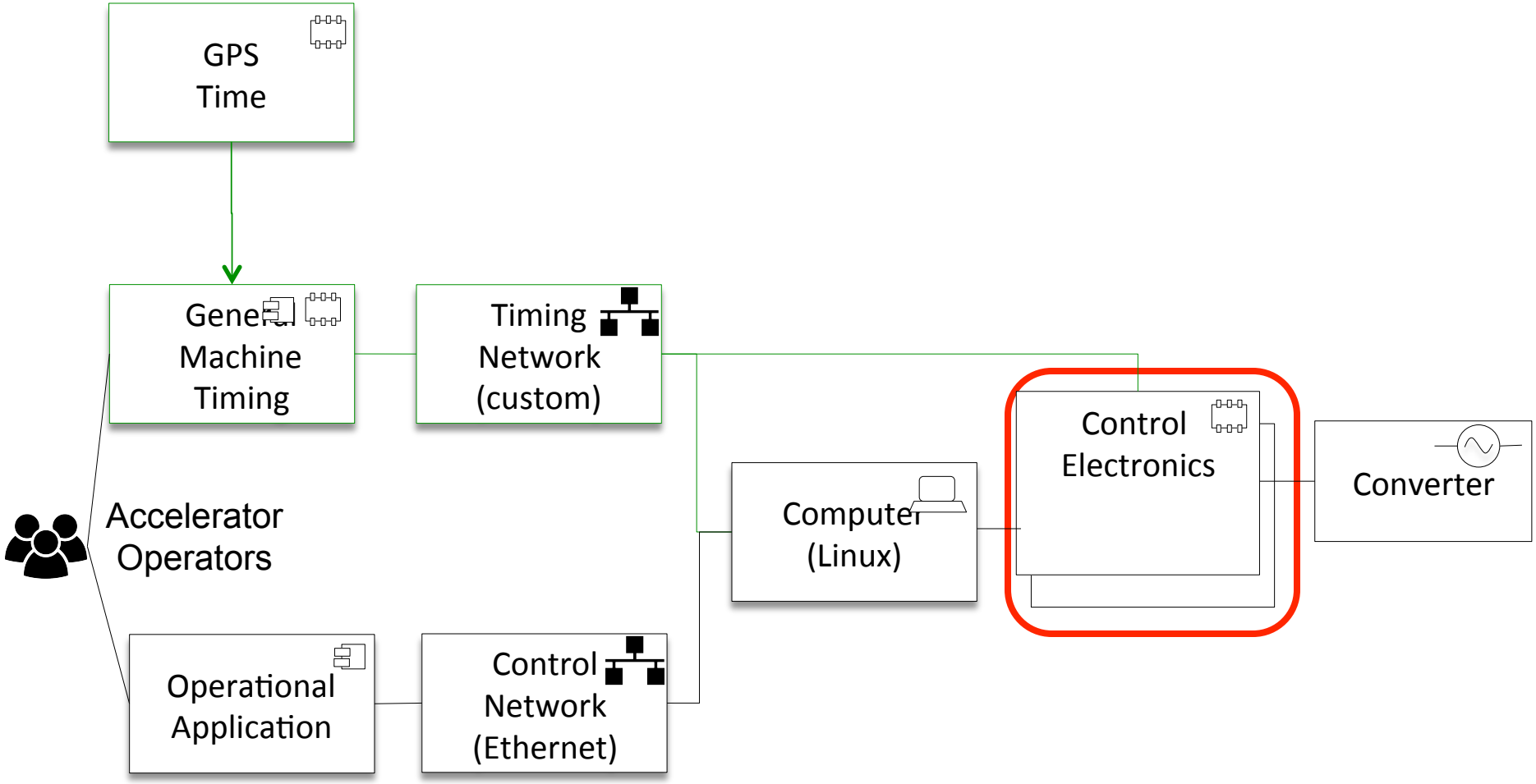
Synchronization and Regulation



All subsystems are synchronized with a common time.

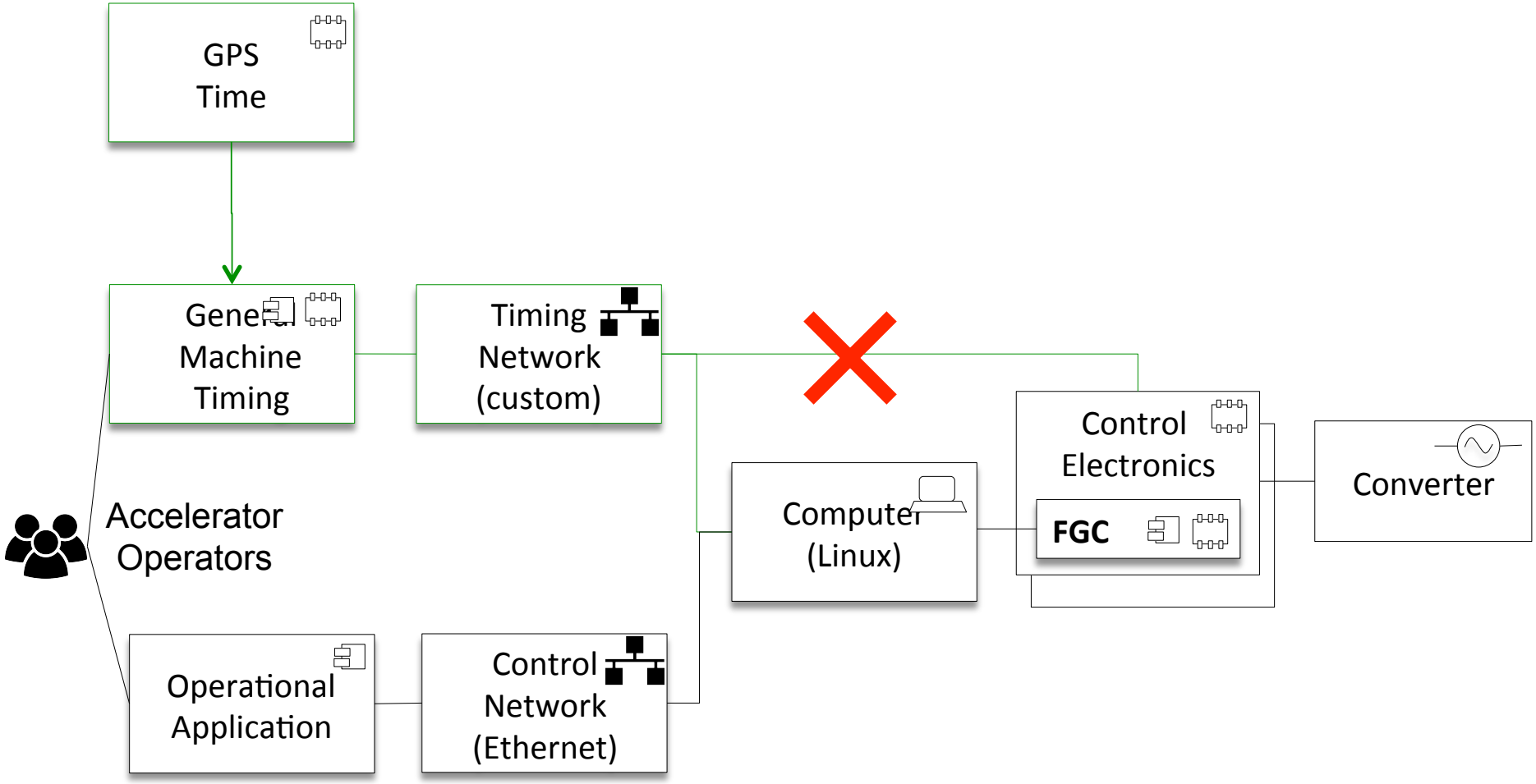
Synchronization: Before 2000

Timing and control networks converged on the front-end and the power converter controller.



Synchronization: Since 2000 (LHC)

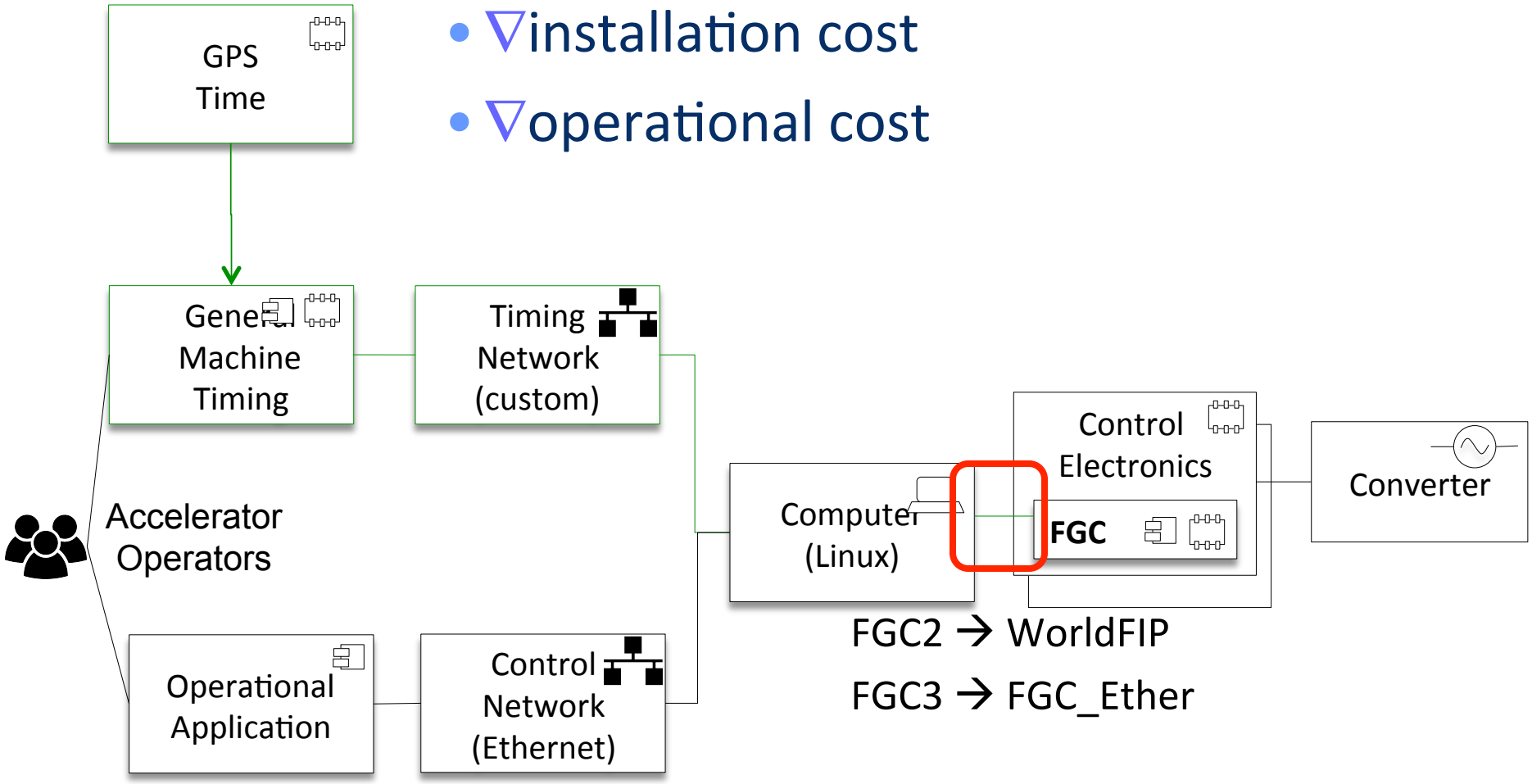
Power converters are controlled by the Function Generation Controller (FGC).



Synchronization: Since 2000

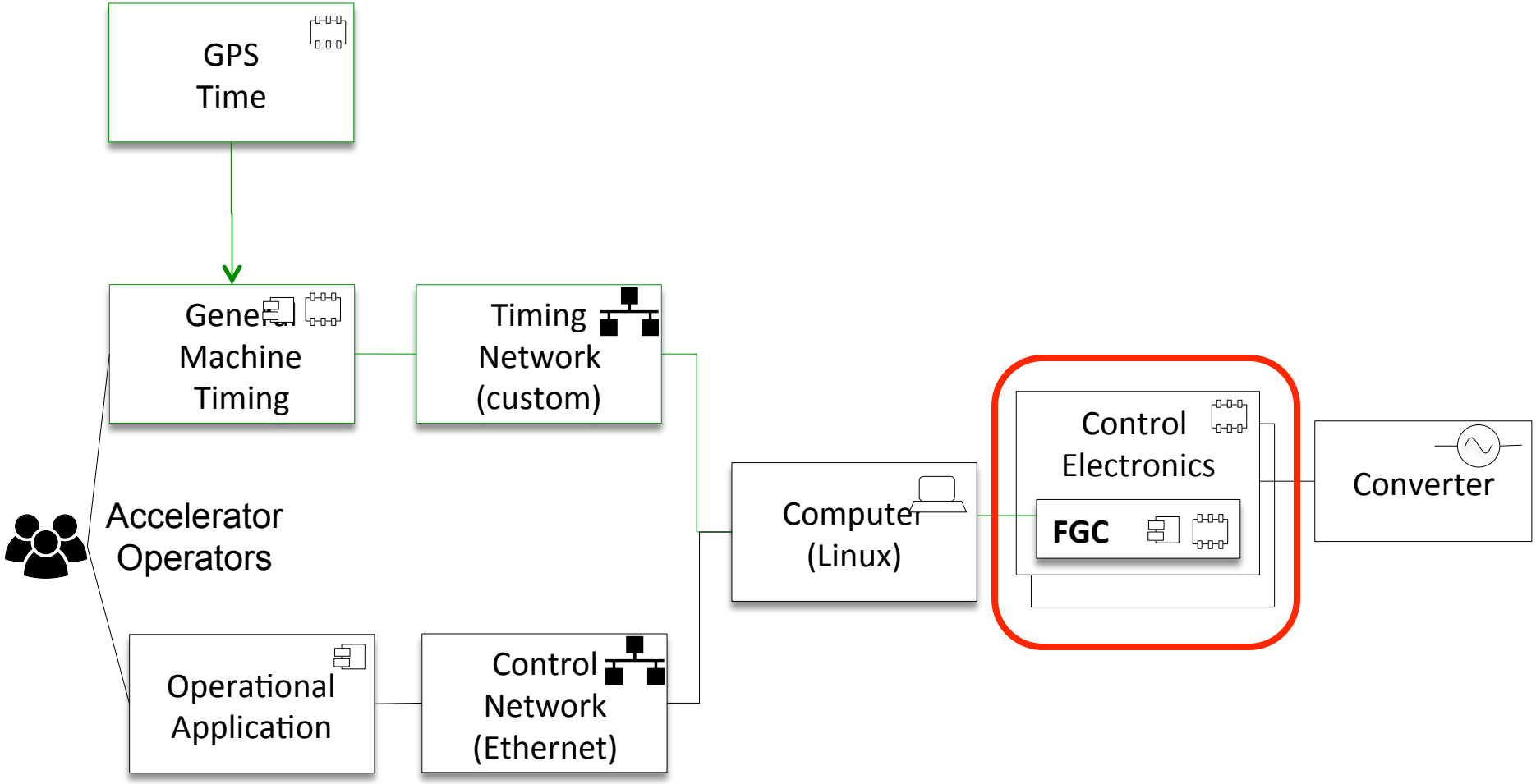
… a standard fieldbus transports timing and control:

- ∇cabling + ∇connectors
- ∇installation cost
- ∇operational cost



Synchronization: Since 2000

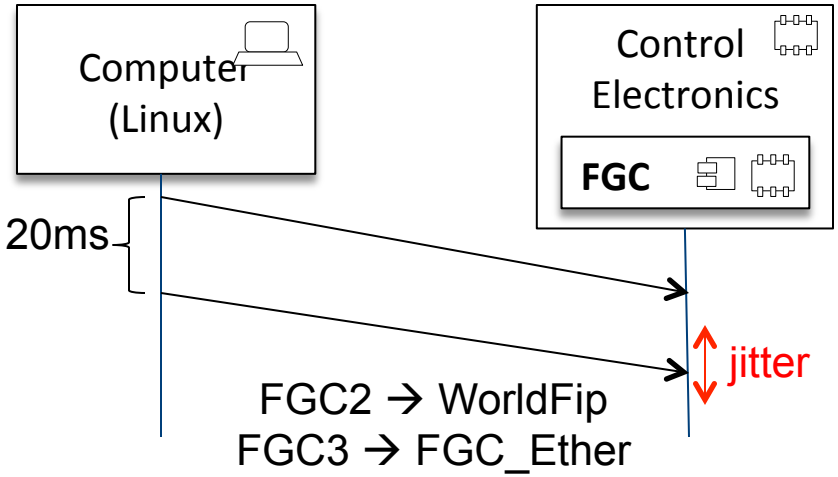
… the FGC needs to recover the time.



Synchronization: PLL

Every 20 ms the front-end broadcasts the time.

This allows the recovery of the machine time with 20 ms precision.



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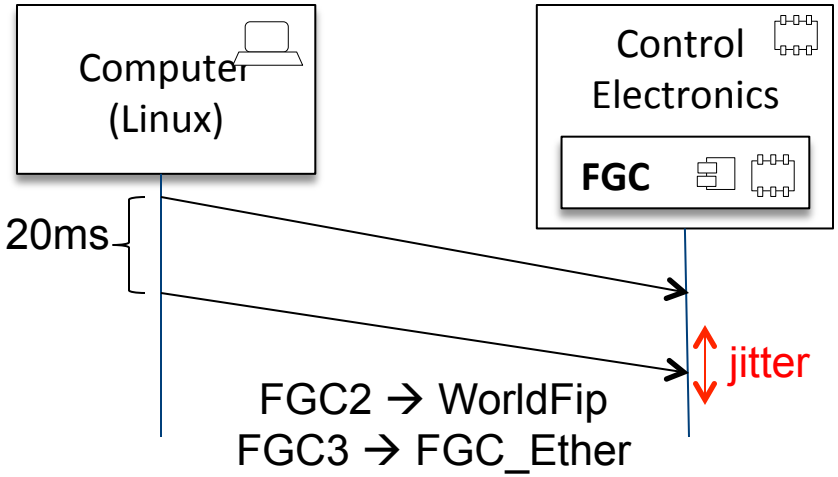
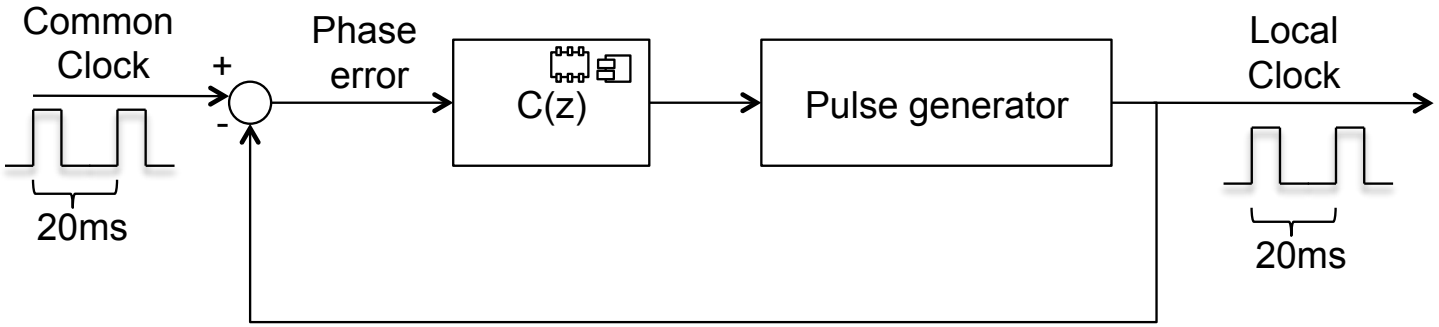


A PLL recovers the 20 ms phase error:

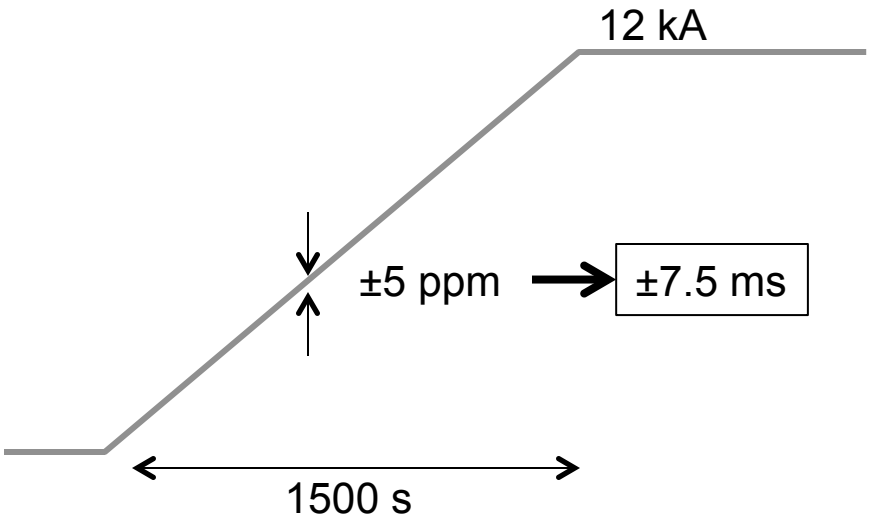


- Overview
- Synchronization and Regulation
- ✓ FGC Phase-Locked Loops

FGC Phase-Locked Loop: Requirements

	FGC2	FGC3
Jitter	1 ms	100 ns
Precision	1 ms	100 ns

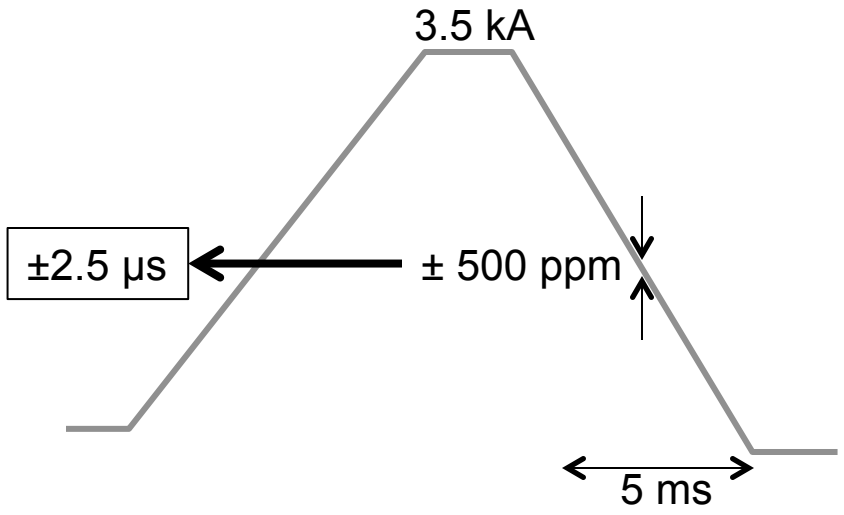
LHC main dipoles current ramp



FGC Phase-Locked Loop: Requirements

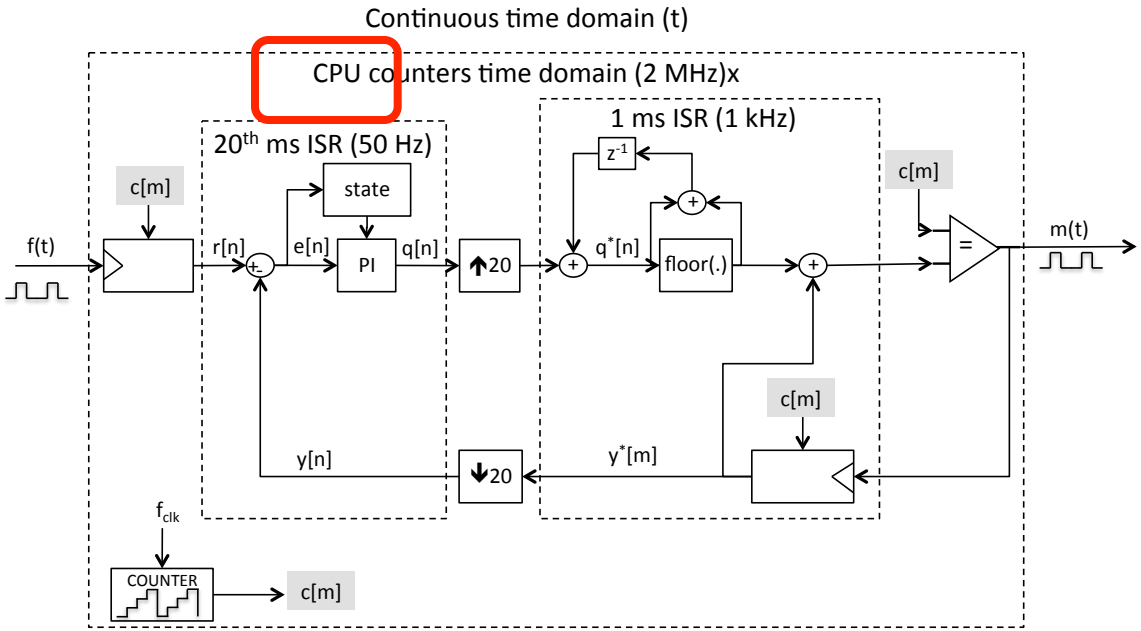
	FGC2	FGC3
Jitter	1 ms	1 µs
Precision	1 ms	1 µs

Linac4 to Booster injection converters



FGC Phase-Locked Loop: Design

	FGC2	FGC3
PLL algorithm	CPU counters Software	50 Hz sync FPGA counters VCXO Software



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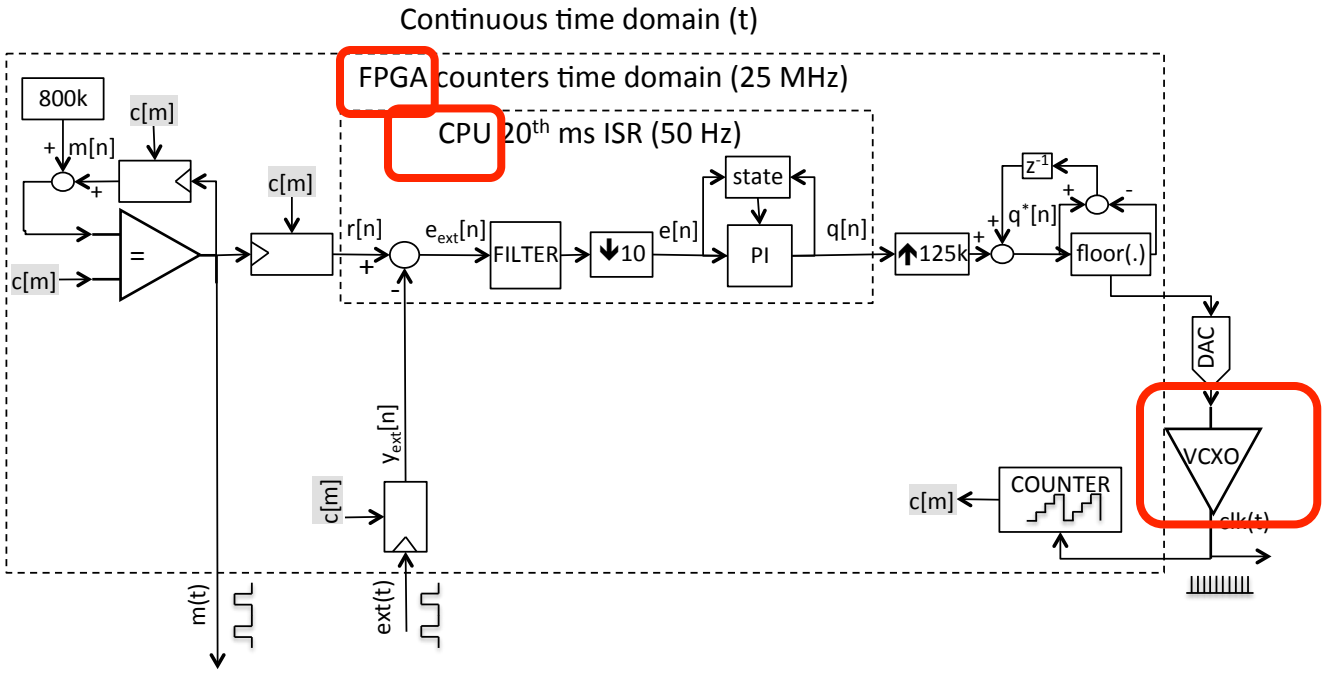
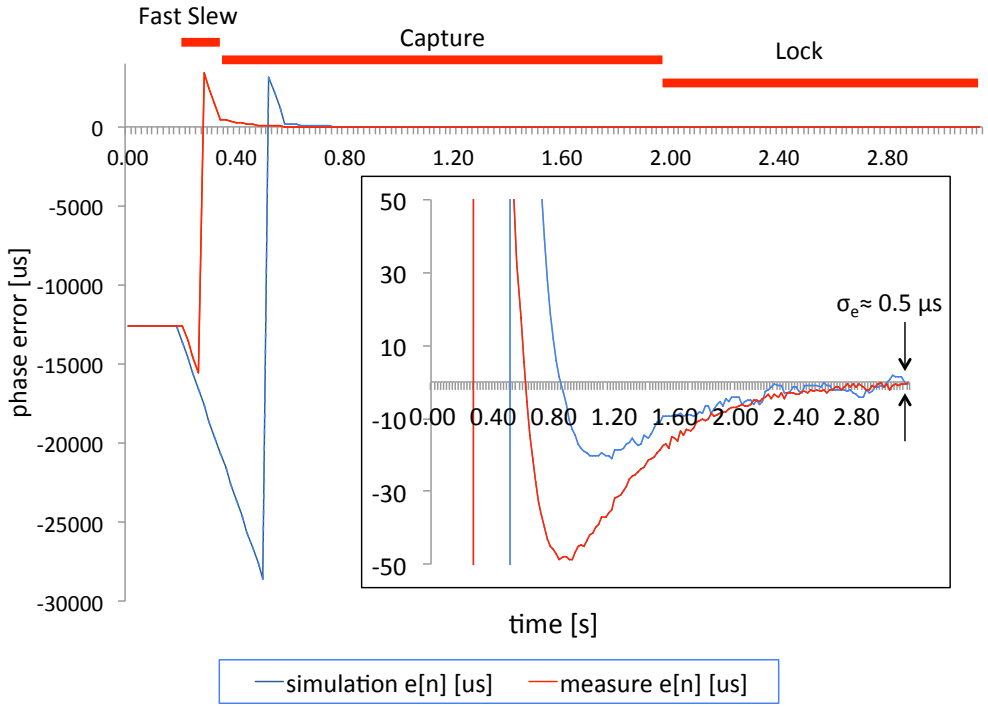


FGC Phase-Locked Loop: Performance

	FGC2	FGC3
Phase error	σ_e=0.5 µs	σ_e<40 ns
Precision	<10 µs	<2.5 µs
Lock Time	<3s	<3s



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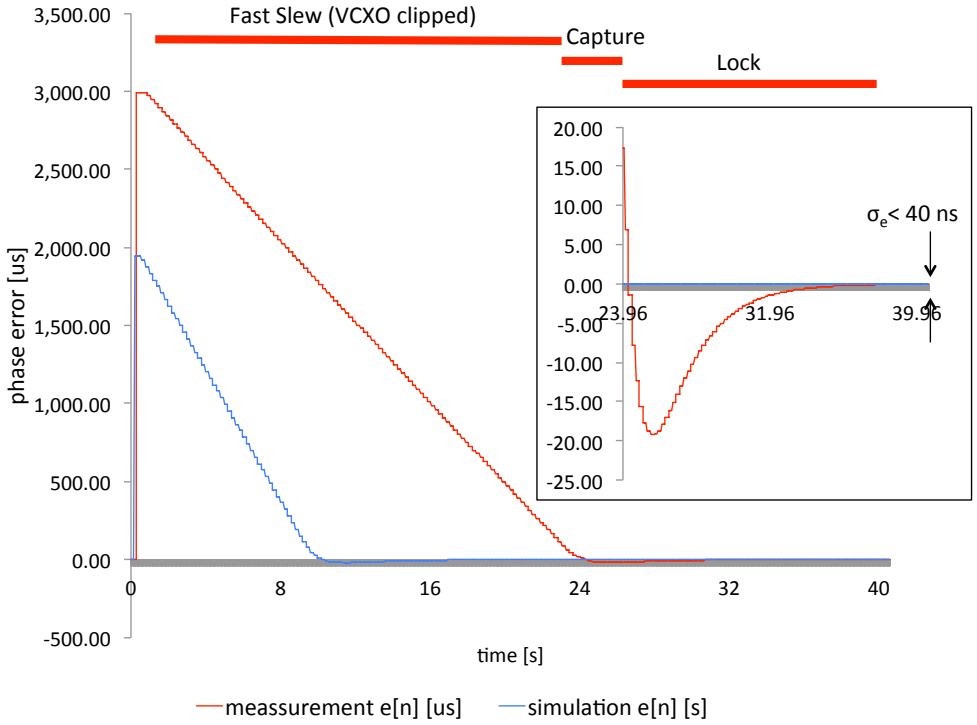

Summary

- Synchronization is needed for:
  - Diagnostics (logging, post-mortem, etc.)
  - Supervisory control
  - Regulation
- Fieldbus can be used to transport timing and control info
- FGC PLL achieved the required performance


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