Message Signalled Interrupts in Mixed-Master Control

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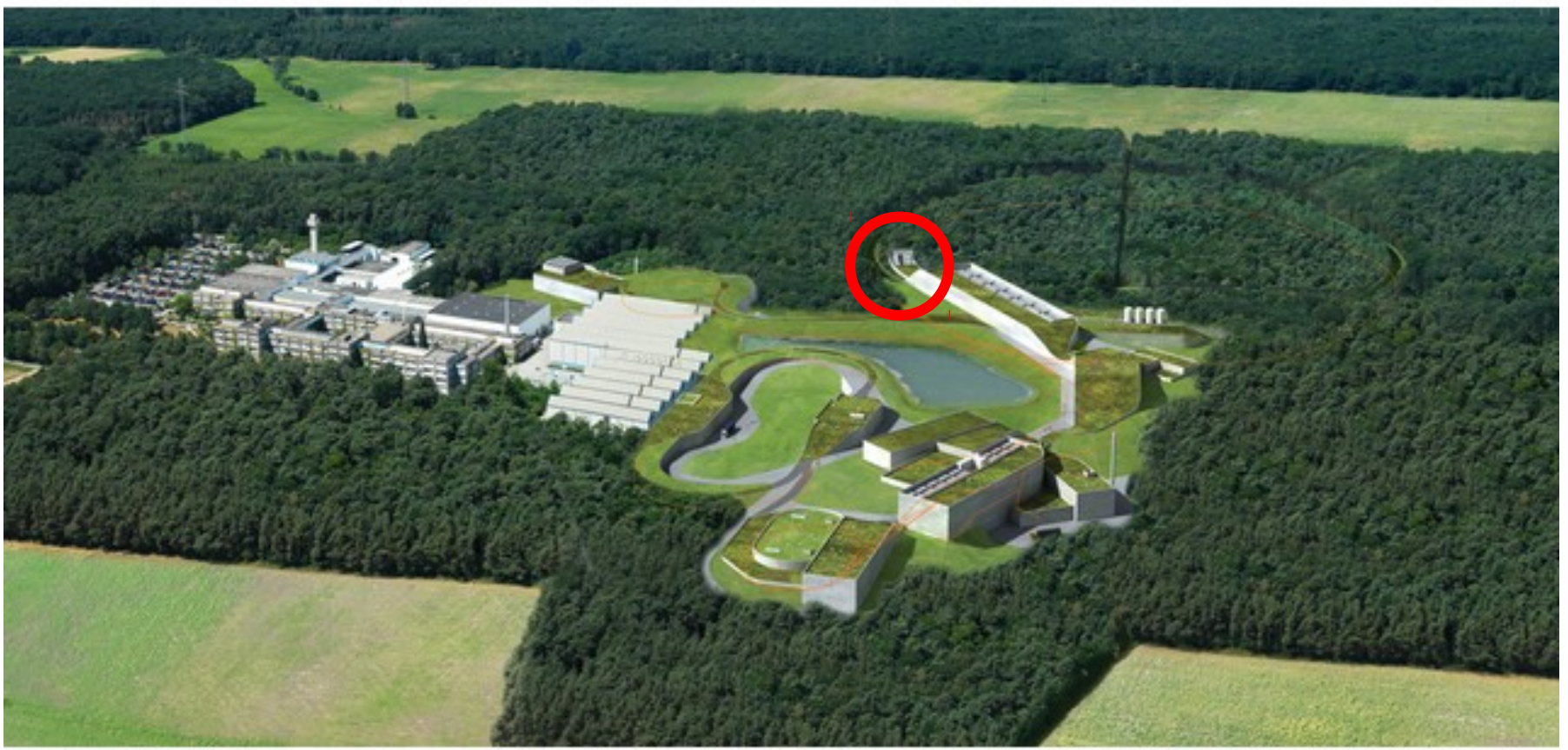
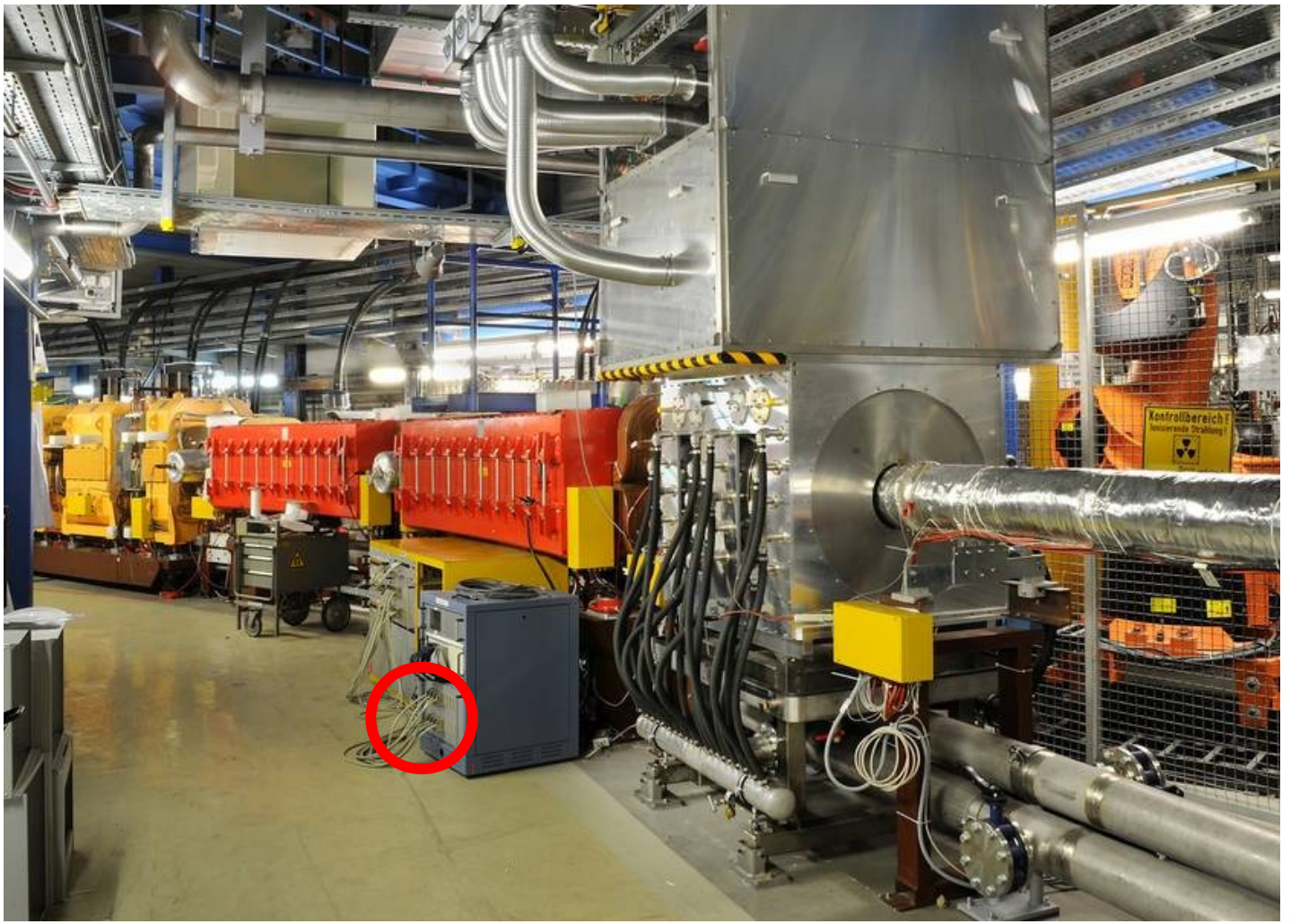
ICALEPCS 2015

What is FAIR?

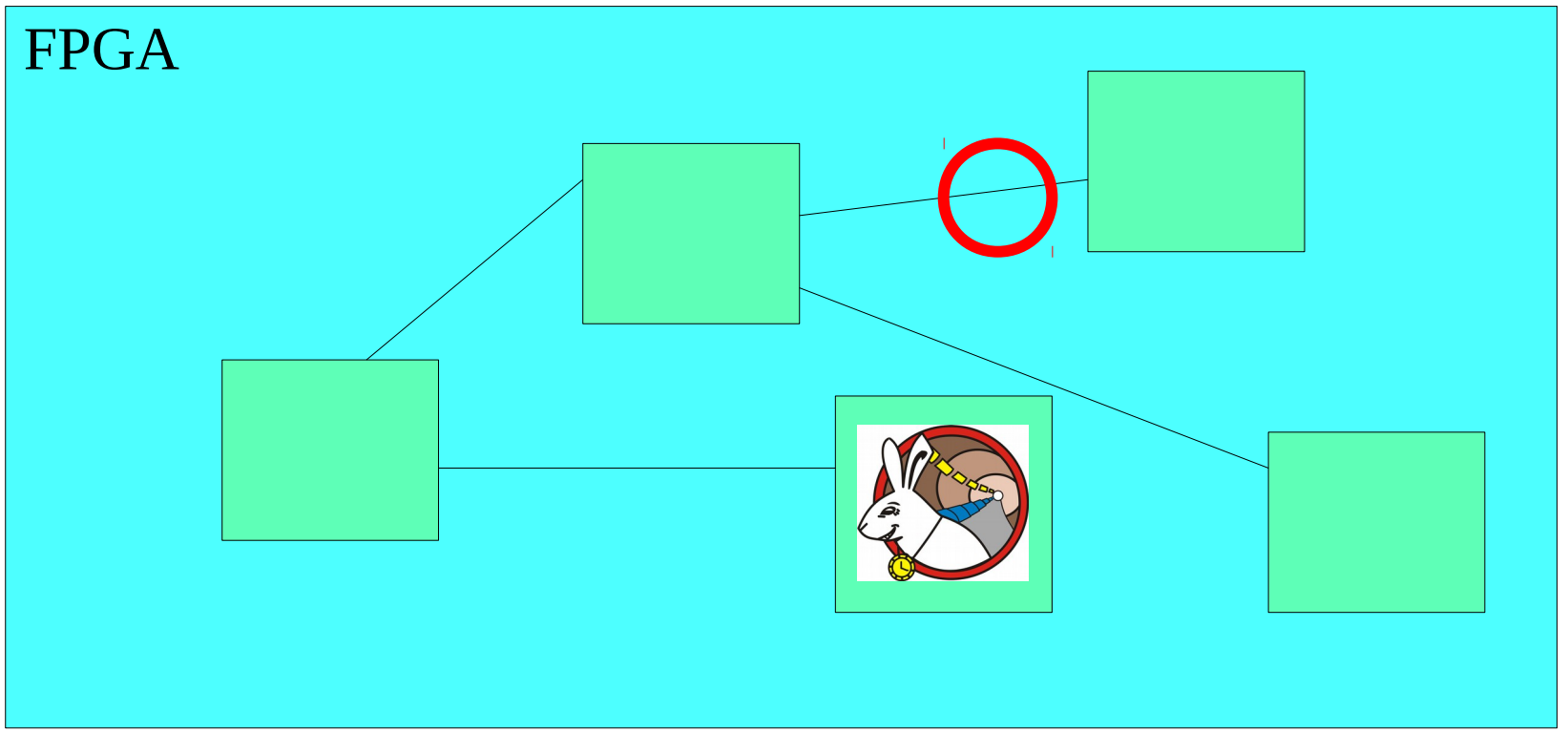


Where is the ring?



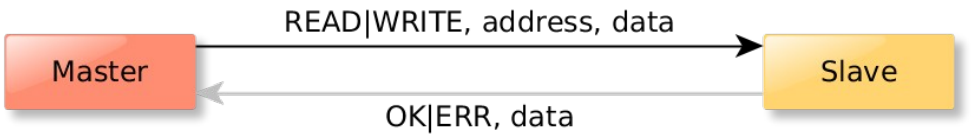
What controls it?

What is inside it?



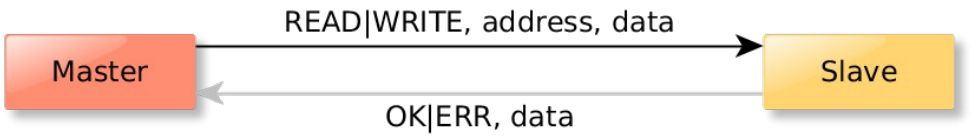
- This talk: the links between cores

What is Wishbone?



- Wishbone: synchronous parallel bus
- Simple master-slave connections only

What is Wishbone?



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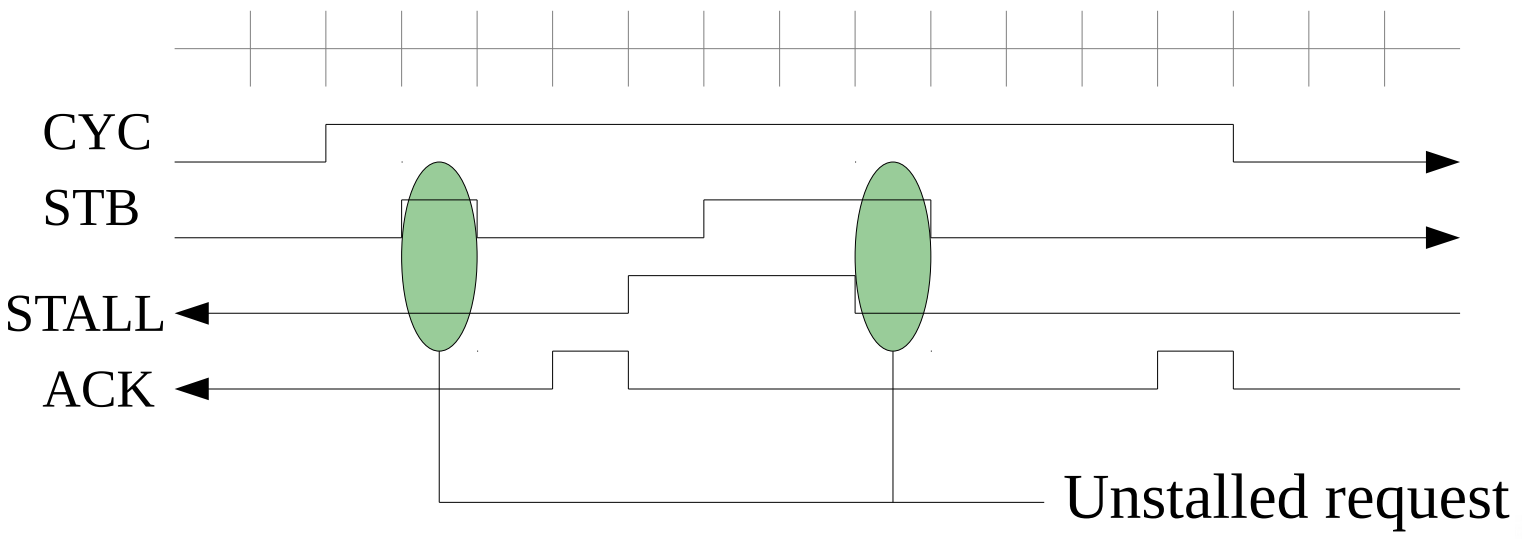
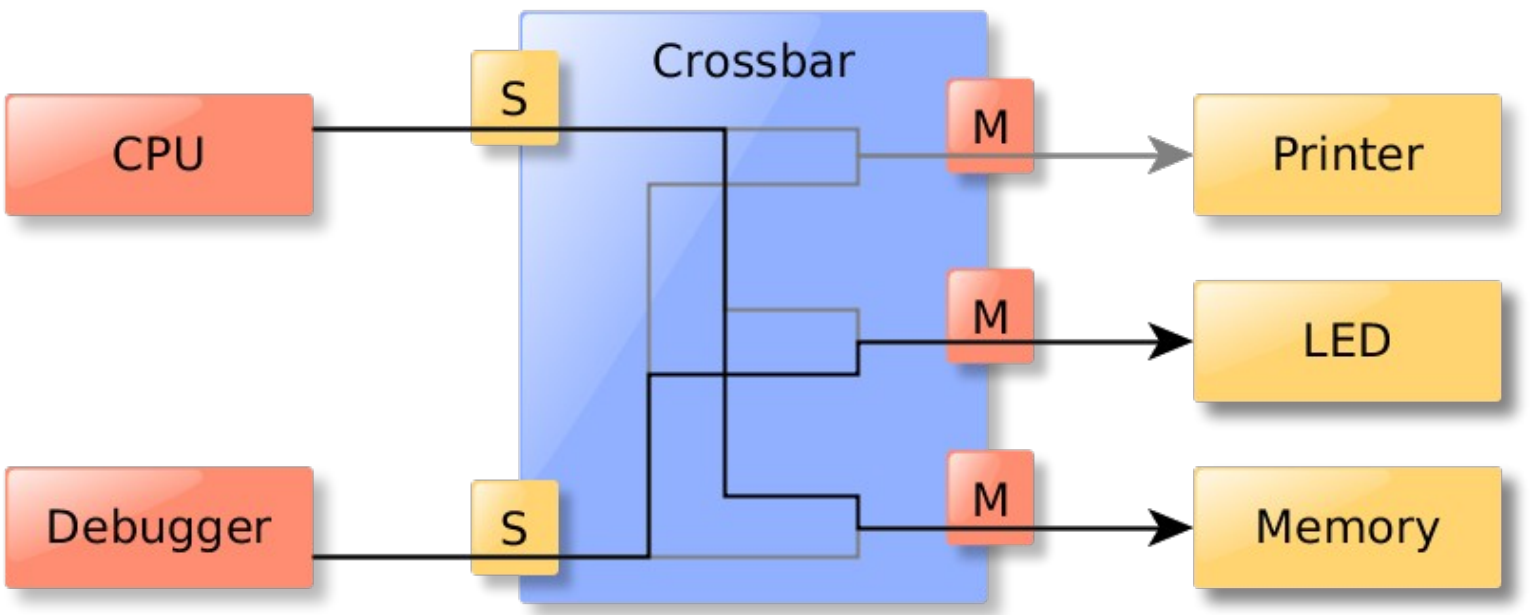


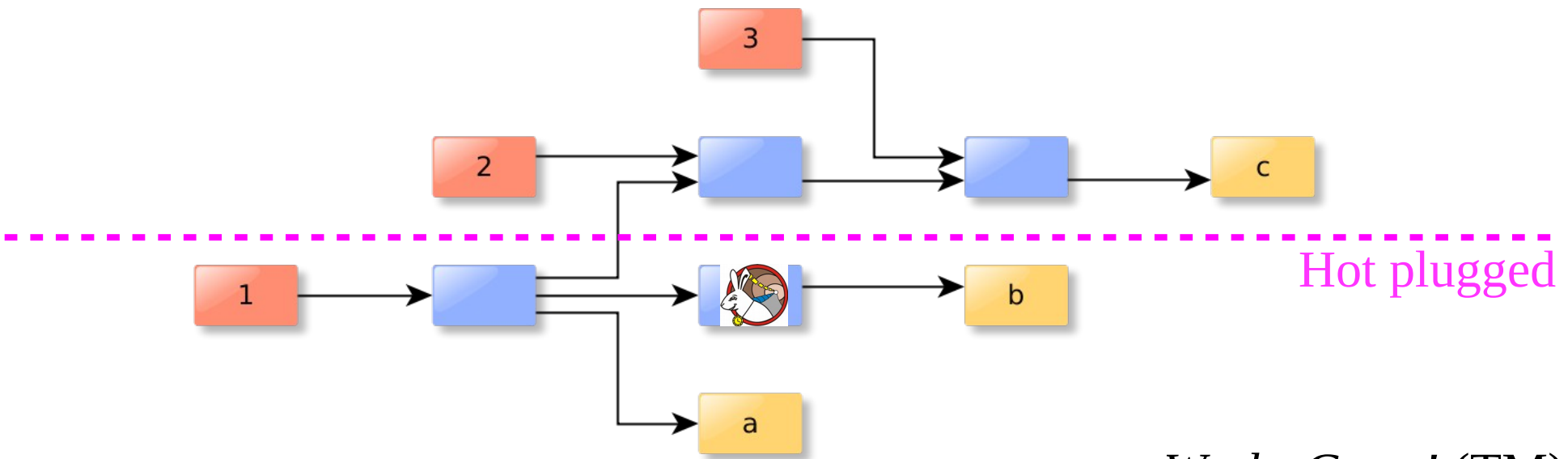
WB bus is extended using crossbars

- A crossbar acts as a network switch
- Slave ports for masters and master ports for slaves



Big systems have multiple crossbars

- Our timing receivers contain ~50 WB components
- Nesting crossbars is a useful organizational tool



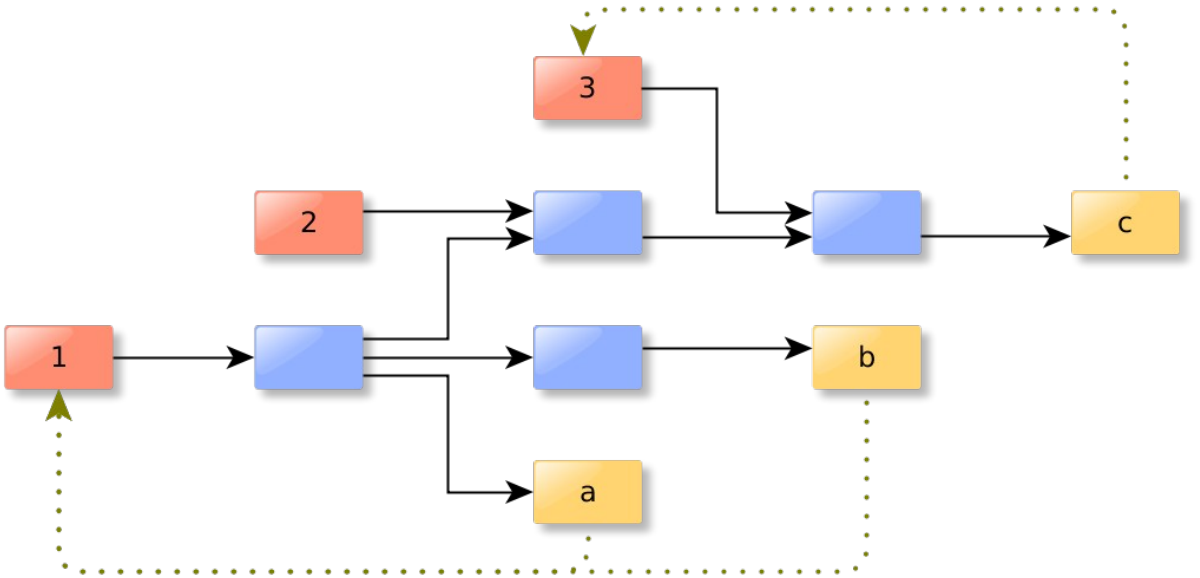
Works Great! (TM)

What's the problem?

- In Wishbone, all communication initiated by master

- Sometimes slaves must tell the master they have data
  - Help! I'm on fire!

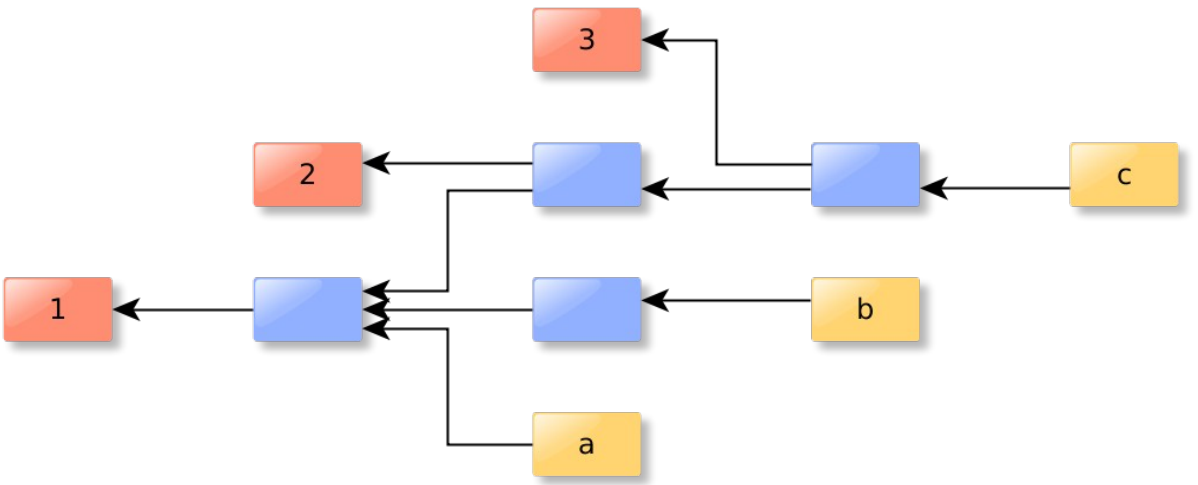
Approach: Classic interrupts



- Slaves connected to a predetermined master
- Interrupt priorities fixed at design-time (shared line)
- Master must query all slaves to find source

➔ Cheap, but ... Not composable

Approach: Message Signalled (MSI)



- Invert Wishbone bus
  - Slaves send messages to masters
  - Address selects master

Requirements for Using MSI

- MSI-enabled masters provide
  - A slave link to the MSI bus
  - A range of addresses to receive MSIs
    - potentially with different priority queues

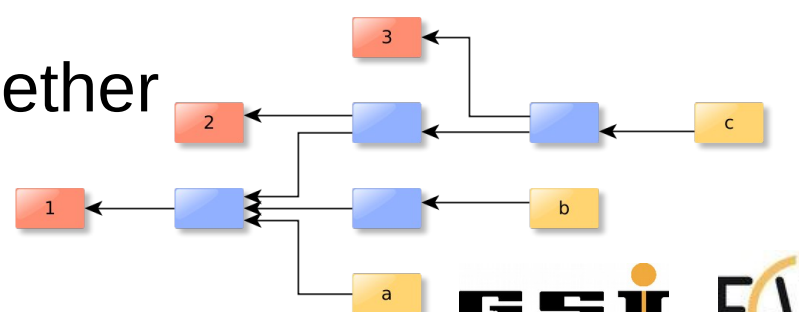
- MSI-enabled slaves provide
  - A master link to the MSI bus
  - For each type of MSI message (burning / ready / full)
    - A register to select which address receives it
    - A register to enable the MSI

MSI is composable

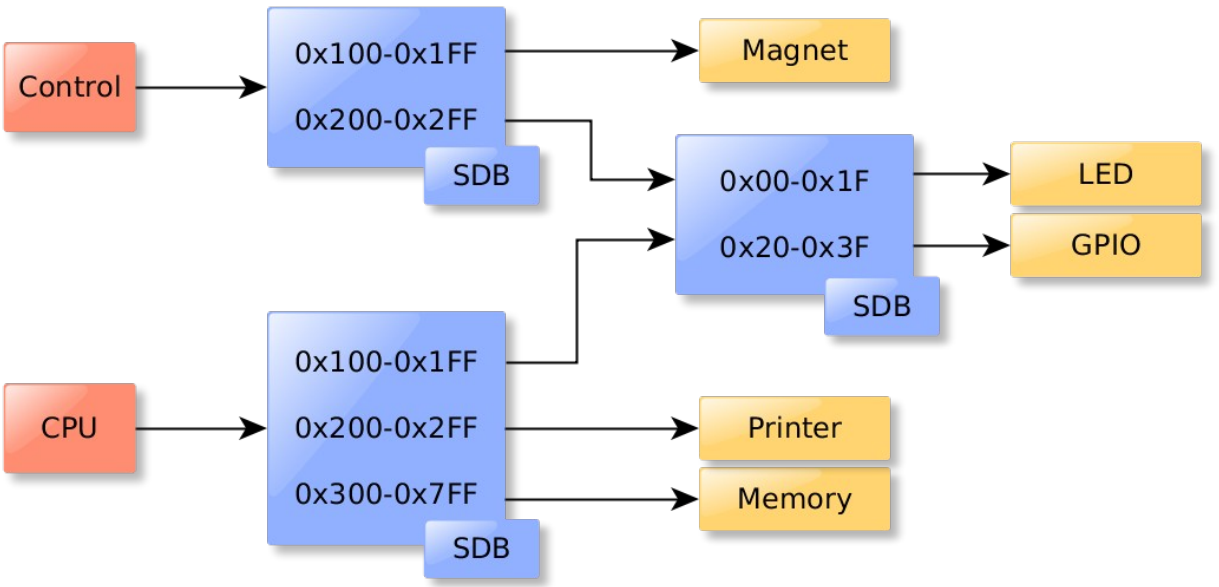
- Masters set address in slave's MSI target address register
  - ➔ Slaves can notify any master which controls them

- Masters have thousands of “interrupt target addresses”
  - ➔ Can immediately distinguish source of MSI
  - ➔ Can prioritize MSIs by choosing destination queue

- Composable: plug crossbars together

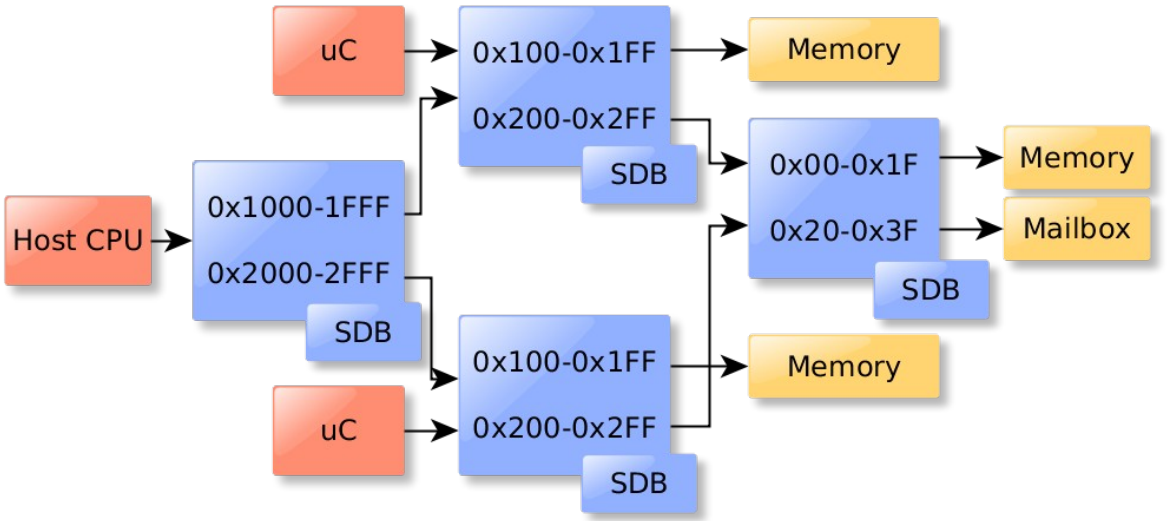


Addressing and SDB



- To find slaves, masters recursively search SDB
- Slaves addresses differ as seen from different masters
- Addresses describe a path, not a destination

Addressing and SDB



- In MSI bus, master address differs from slave PoV
- When masters scan bus, also scan backwards path
  - → address slaves need to send master MSI
  - → constructed bottom-up

WB+MSI well suited for complex buses

- Wishbone scales well, from 2- to 50-component systems
- MSI expands bus composability to interrupts
- SDB must be extended with master records

Questions?