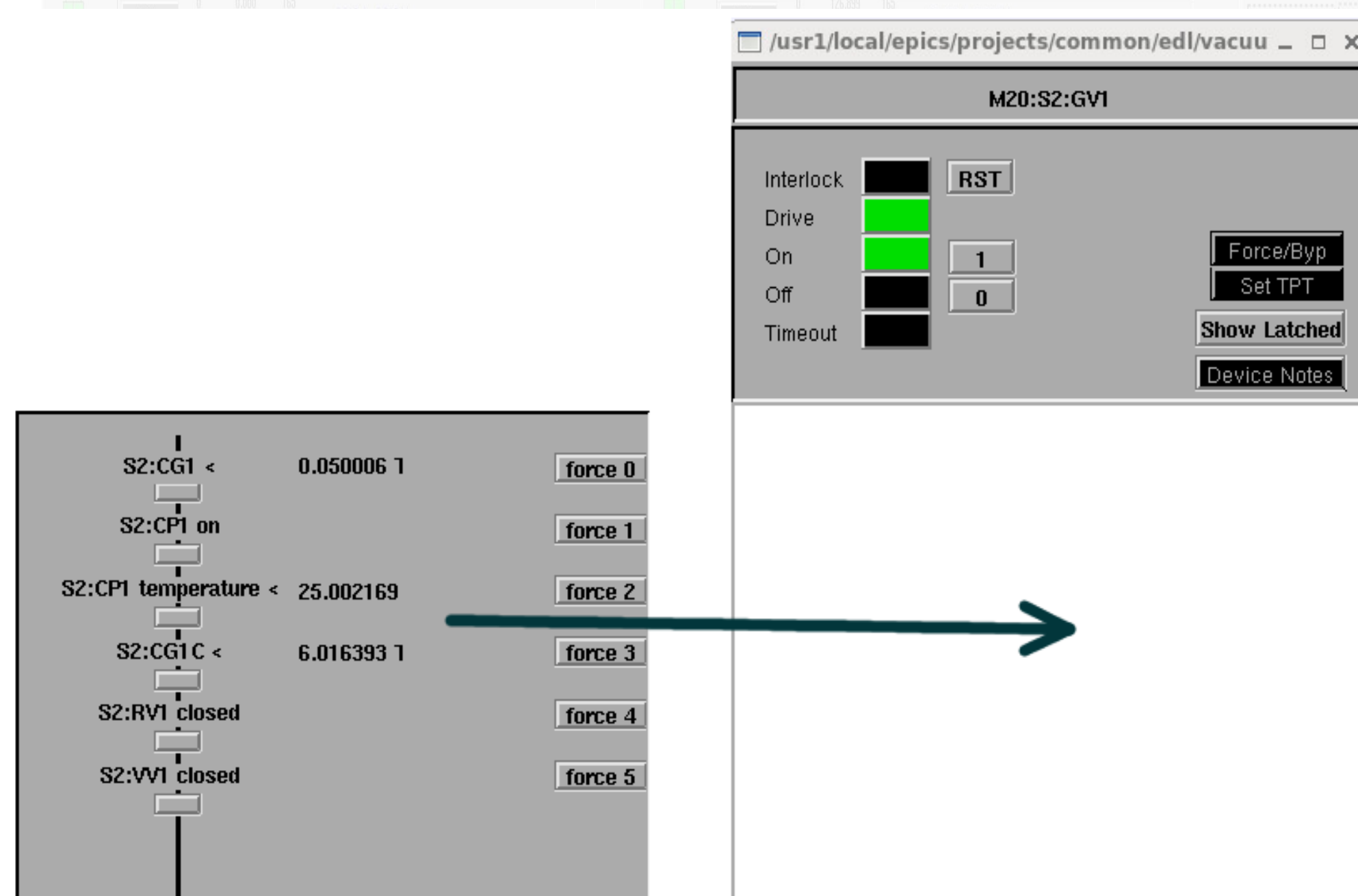


Abstract

The control system for TRIUMF's upgraded secondary beam line M20 was implemented by using a PLC and one of many EPICS IOCs running on a multi-core Dell server. Running the IOC on a powerful machine rather than on a small dedicated computer has a number of advantages such as fast code execution and the availability of a large amount of memory. A large EPICS database can be loaded into the IOC and used for visualization of the interlocks implemented in the PLC. The information about interlock status registers, text messages, and the names of control and interlock panels are entered into a relational database by using a web browser. Top-level EPICS schematics are generated from the relational database. For visualization the embedded windows available in the Extensible Display Manager (EDM) are the EPICS clients, which retrieve interlock status information from the EPICS database. A set of interlock panels is the library, which can be used to show any chains of interlocks. If necessary, a new interlock panel can be created by using the visualization tools provided with EDM. This solution, in use for more than 3 years, has proven to be reliable and very flexible.

Control device panel contains embedded interlock panel. All necessary information is retrieved from EPICS database:



Motivations

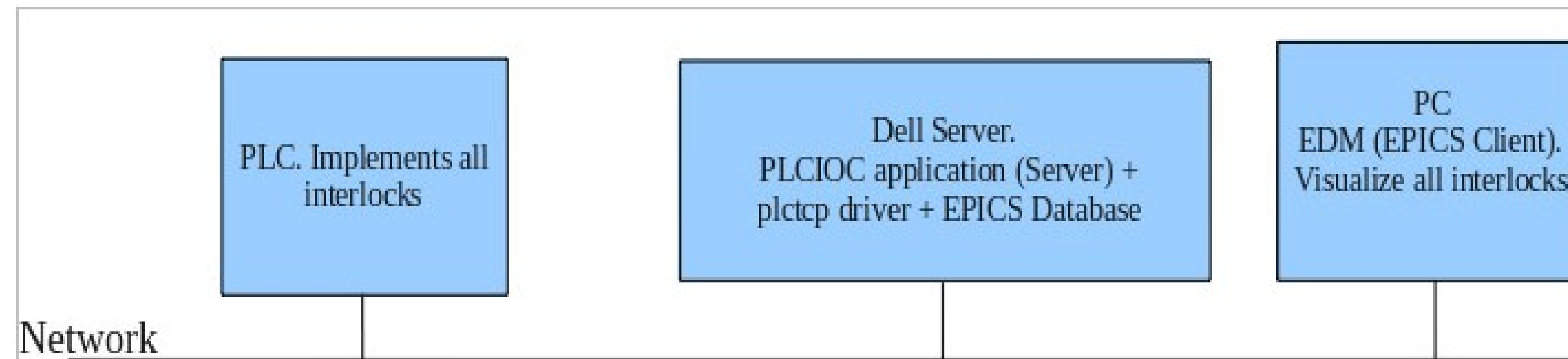
15 years ago we lived in MEGA time: MHz CPUs, Mb Memory, Megabit Ethernet.

Now we live in GIGA time: GHz CPUs, Gb Memory, Gigabit Ethernet.

We can develop much simpler solutions (not 1000 times simpler, though 😊)

The new control systems at TRIUMF are implemented by using the Experimental Physics and Industrial Control System toolkit (EPICS). The M20 Control System contains Programmable Logic Controllers (PLCs) + EPICS.

EPICS support is realized as an application running on a Linux server (PLCIOIC). This application communicates with the PLC on one hand and with the EPICS clients on the other:



A Multi-core Dell PowerEdge R610 is used to host PLCIOIC.

- Memory usage by ~100 devices is 1.5% (of 8 Gb).
- CPU usage is 12% for one core (out of 8).
- Transfer of data between EPICS clients, PLCIOIC, and PLC is provided by a Gigabit network.

All interlocks are implemented in a PLC. The EPICS screens (device control + interlock panels) are used only for visualization of the interlocks.

Rules for construction of Interlock Panel names

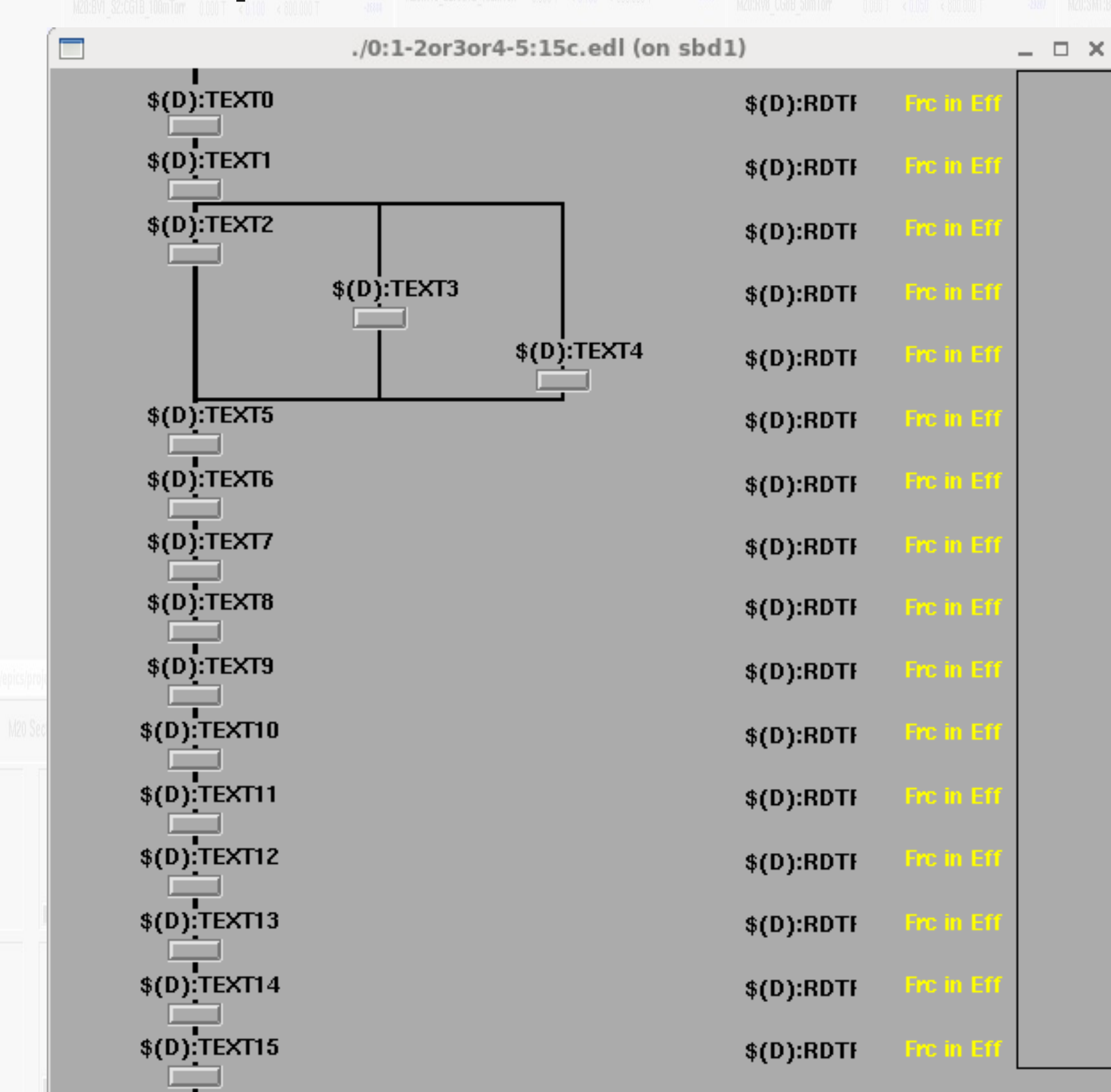
The Interlock Specification provides logical equations for interlocks. Enumeration of bits starts with zero:

(Bit_0 and Bit_1) and (Bit_2 or Bit_3 or Bit_4) and Bit_5 and Bit_6 and ... (some more bits)

Such equations correspond to the ladder logic of the PLC code. The name of the interlock panel is constructed by applying the following simple rules:

- Dash sign represents “and” for groups before and after the sign (corresponds to vertical lines on interlock panels).
- If several bits are used in “and” statements they are combined into the range of bits by using colon sign, for example, 0:1.
- The word “or” is used every time to avoid confusion.

The interlock panel name is:0:1-2or3or4-5:15.edl



Rather complicated hierarchical interlocks can be handled in a simple way:



The visualization scheme is universal: M20 optical and vacuum devices are handled in similar manner:



CONCLUSION

A complete scheme for interlock visualization was created. It was used for 3 years on the TRIUMF M20 Secondary Beam Line and proved to be easily maintainable and extensible. It can be recommended for development of any new control system, which uses the EPICS toolkit.

