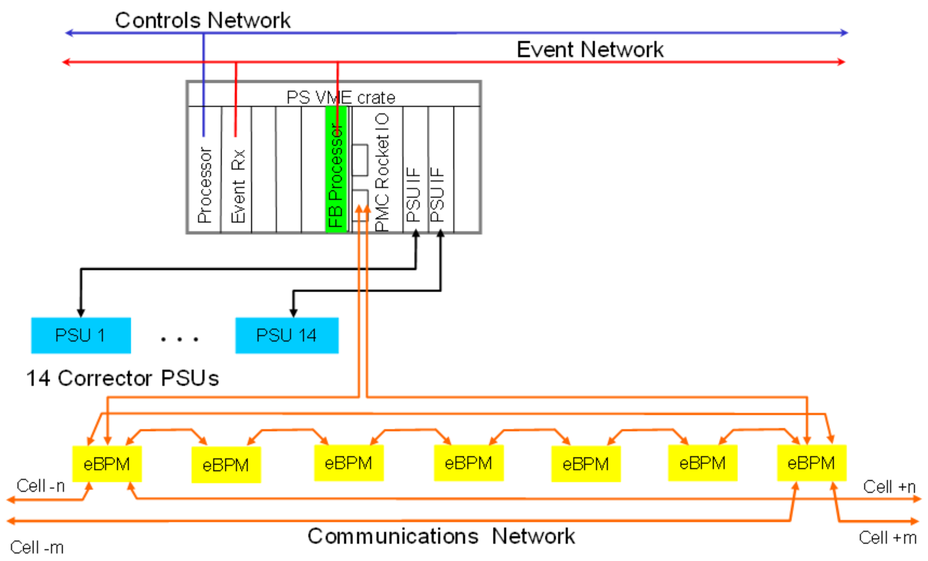
CERN Open Hardware Experience: Upgrading the Diamond Fast Archiver

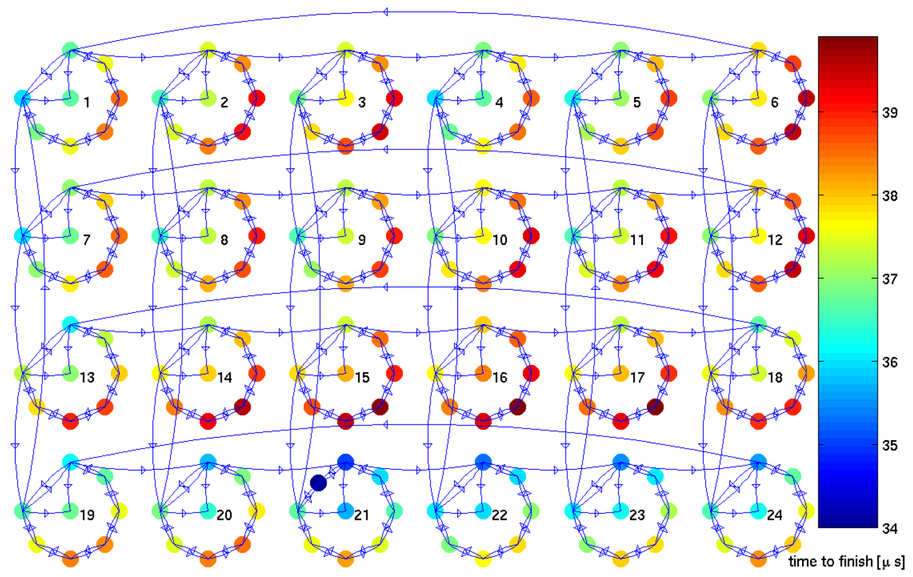
I.S. Uzun and M.G. Abbott
Diamond Light Source, Oxfordshire, UK

Diamond FOFB Architecture



The system architecture for the FOFB for a single Storage Ring (SR) cell consists of 7 EBPMs, a PMC receiver, VME feedback processor and power supply controllers. Diamond SR consists of 24 cells.

Diamond Communication Network



All Storage Ring EBPMs and PMC Receivers are connected to Communication Network in 2D Torus topology.

The Fast Acquisition Archiver

The FA archiver captures X,Y position data from a network of EBPMs and other sources at 10 kHz, maintains a rolling historical record and rebroadcasts the complete data stream to all interested parties. Other sources contributing to the network are a handful of X-ray BPMs and power pick-ups from the RF cavities.

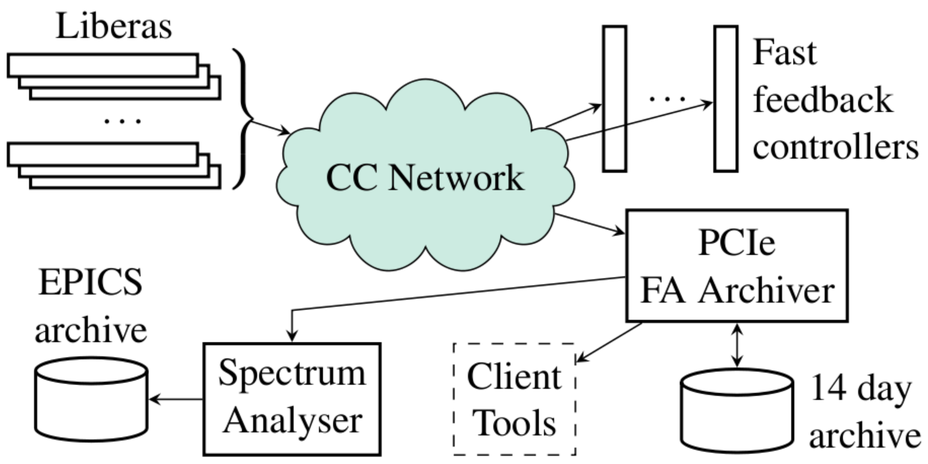
- 512 X,Y position updates every 100 μs, sustained 40 MB/s.
- At Diamond we archive the last 14 days of orbit position.
- Any number of clients (limited by network connection to archive server) can read the archive and subscribe to the rebroadcast live data stream.

Hardware Requirements for FA Archiver

Implementation of FA archiver interface requires a PCIe form factor hardware platform with following on-board resources:

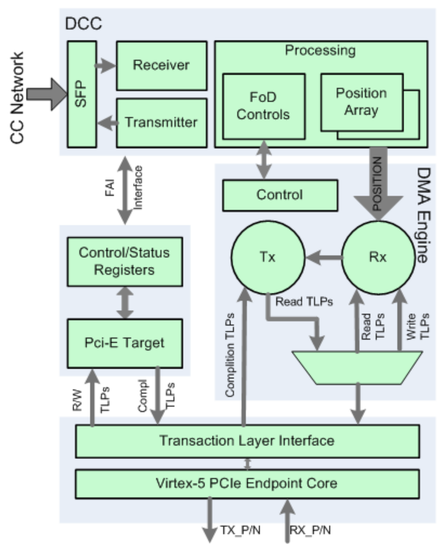
- Minimum 1-lane of PCIe bus interface. This could be either through dedicated IPs blocks on an FPGA device or a bridge chip external to the FPGA.
- At least 1 MGT on the FPGA for DCC implementation.
- On-board SFP connector(s) for physical connection to the communication network.
- Clocking resources required for PCIe, DMA data transfer and DCC FPGA logic.

FA Archiver in Context



The FA archiver acts as a passive listener and makes the FA data freely available.

Existing Firmware Design on ML555 Card

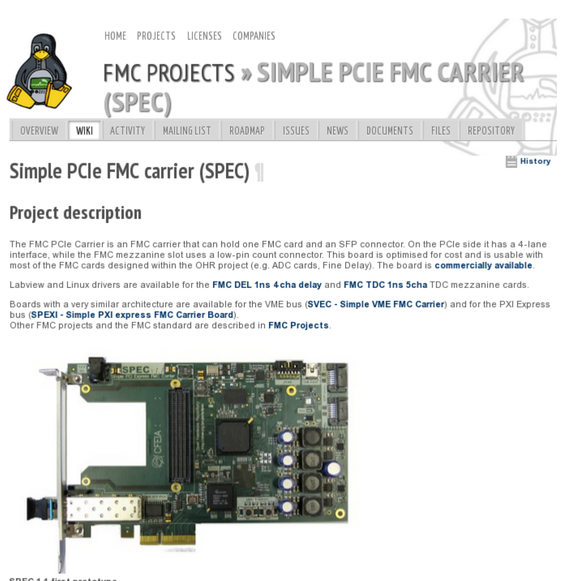


- Integrates the DCC into a bus master PCIe architecture on the ML555 FPGA board.
- Target logic is responsible for capturing memory write and memory read PCIe Transaction Layer Packets (TLPs) for control and status register access.
- The DMA initiator logic generates memory write TLPs to transfer 4K byte frame data from the DCC core to the host system memory through PCIe endpoint.

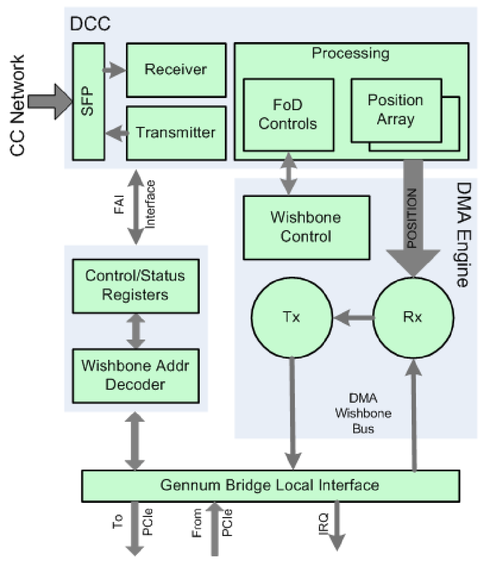
Motivation

- To address obsolescence of the existing Xilinx ML556 PCIe platform.
- To move to an open platform for continuing support in the community.
- To get familiar with Open Hardware initiative, and build experience with the inner workings of the repository.

FA Archiver Interface on SPEC Card



SPEC 1.1 first prototype



By studying the open-source schematics and reference firmware design available on the repository, we were able to identify the modifications to be taken towards implementing the FA Archiver on the SPEC card.

- PCIe Interface uses on-board Gennum PCIe bridge.
- Clocking Resources uses on-board programmable oscillator for Communication Controller.
- SoC Communication uses Wishbone bus.

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