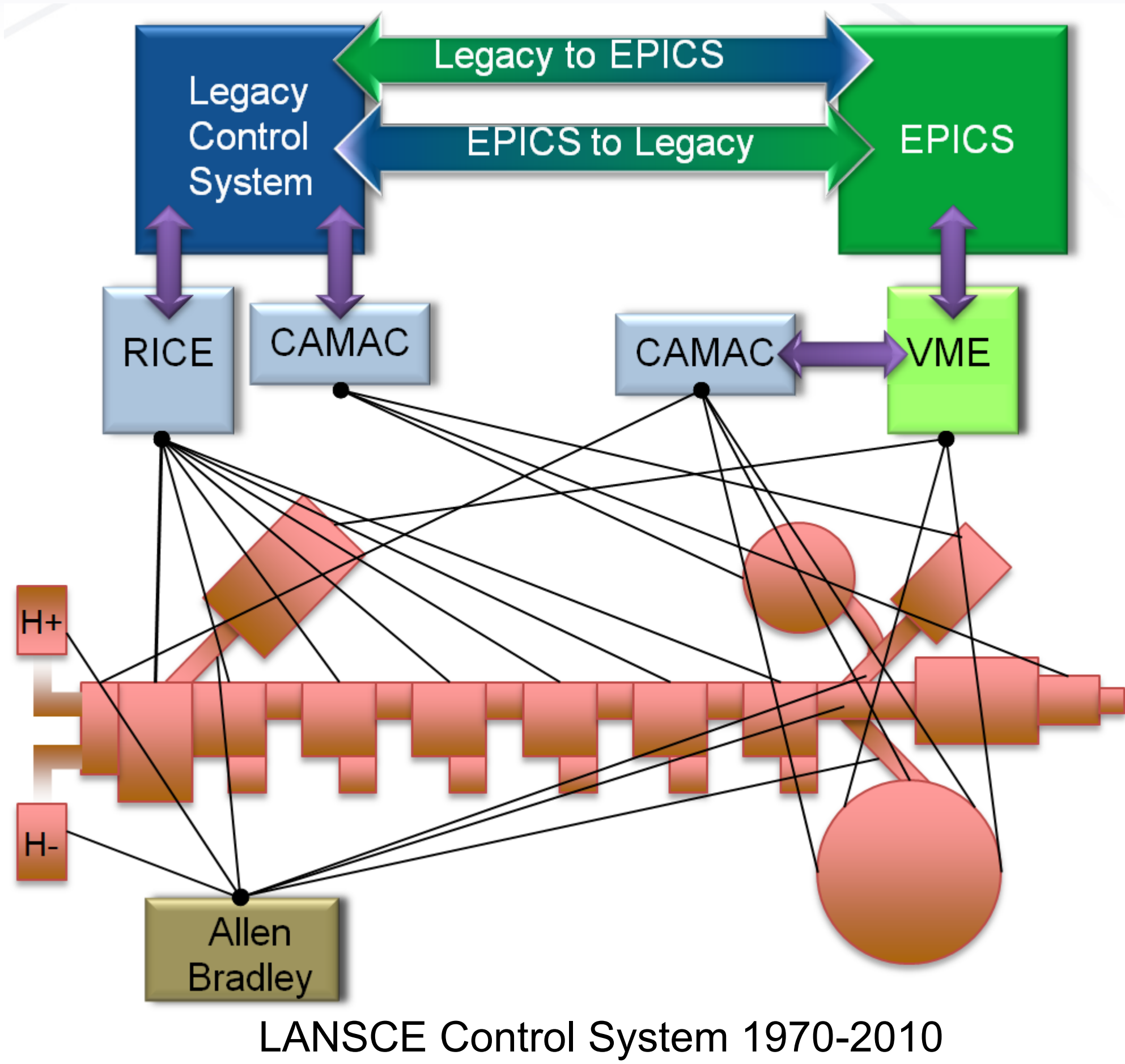


LANSCE CONTROL SYSTEM UPGRADE STATUS AND CHALLENGES*



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LANSCE Control System 1970-2010

The LANSCE accelerator looks back at almost 45 years of operations. It was one of the first using computer technologies to control and monitor its beam line components. It started out with a custom in-house design called RICE (Remote Instrumentation and Control Equipment) which was installed in the early 1970's when the facility was built. Since then the facility has seen partial upgrades and extensions utilizing CAMAC, VME, and PLCs while introducing EPICS (Experimental Physics and Industrial Control System) in the 1990's as supervisory software control application. The monumental challenge of upgrading the control system is focused around the need to replace our VAX based legacy control system which goes hand in hand with our RICE system.



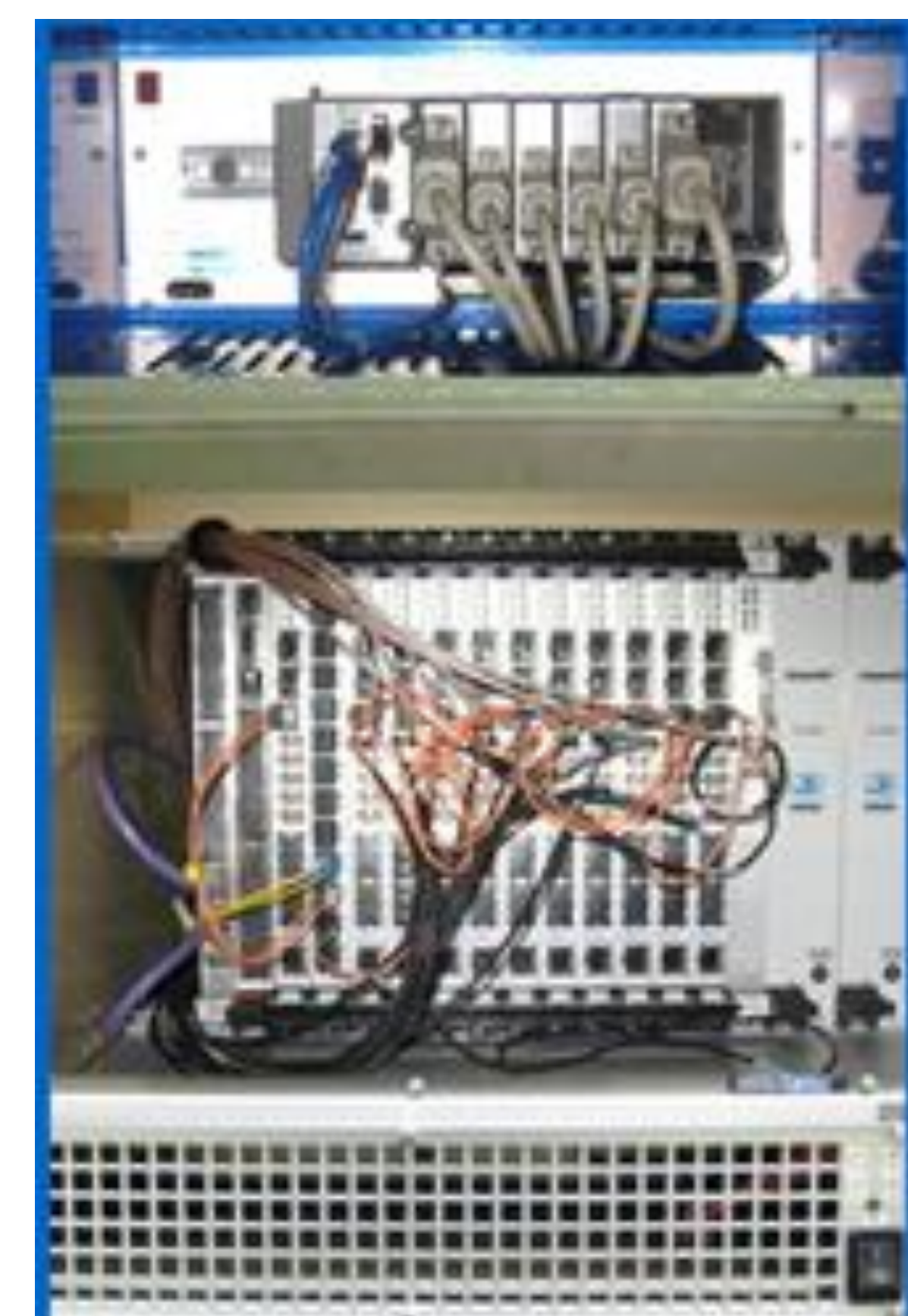
2010
Fiber Optics Network
cRIO



National Instrument CompactRIO (cRIO): reconfigurable control and acquisition system supported by EPICS. Real-Time Controller with 8-slots chassis and a user programmable Xilinx Virtex-5 LX110 FPGA) in the backplane interfacing to signal conditioning modules.

Master Timer

The new Timing Pattern Generator (TPG) is a dual-redundant system. Each of the redundant TPG's has a VME-64x crate, a MVME-6100 processor, a set of Micro Research Finland (MRF) event-generator modules, and an AC zero-crossing detector and beam-enable logic module (implemented in a cRIO system). The cRIO FPGA-based beam enable logic has been used to implement specific features, such as enabling or disabling a beam from the operator consoles, single-shot mode, single-burst mode, continuous-burst mode, burst of bursts mode, and cycle stealing.

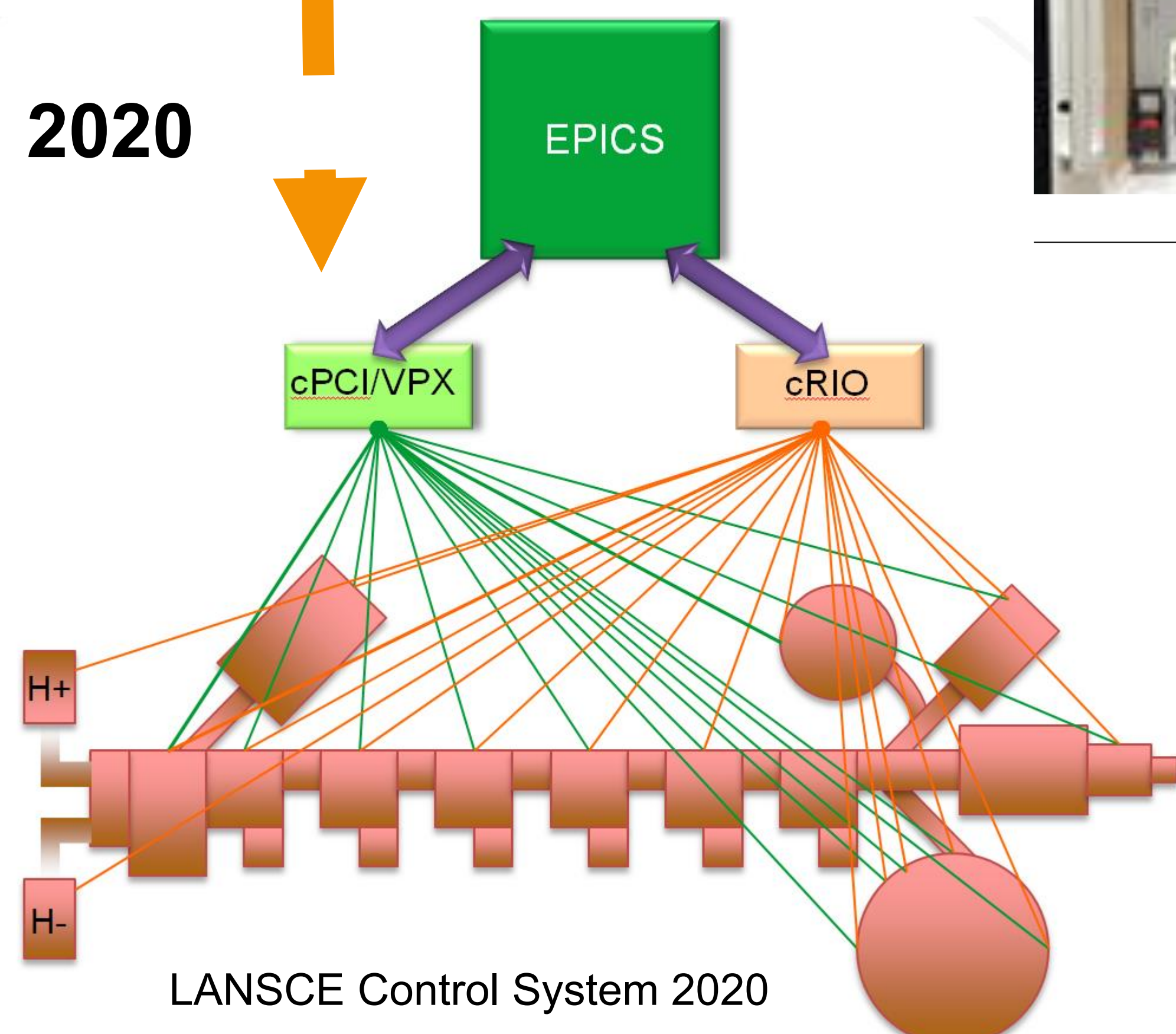


2015
cPCI/VPX

Current Upgrade Status

	RICE to Industrial Controls	RICE to Synchronized Data Acq.	BPPMs	Wire Scanner	CAMAC to cRIO	HARP	Emittance
Total Number of Systems to be upgraded	66	66	34	53	38	32	3
Upgrades Installed / In Production	9	0	0	4	28	1	0
Equipment on Hand but Not Installed	27	31	7	8 (40)	2	0	1
Remaining Systems to be Purchased	30	35	27	41 (9)	8	31	2

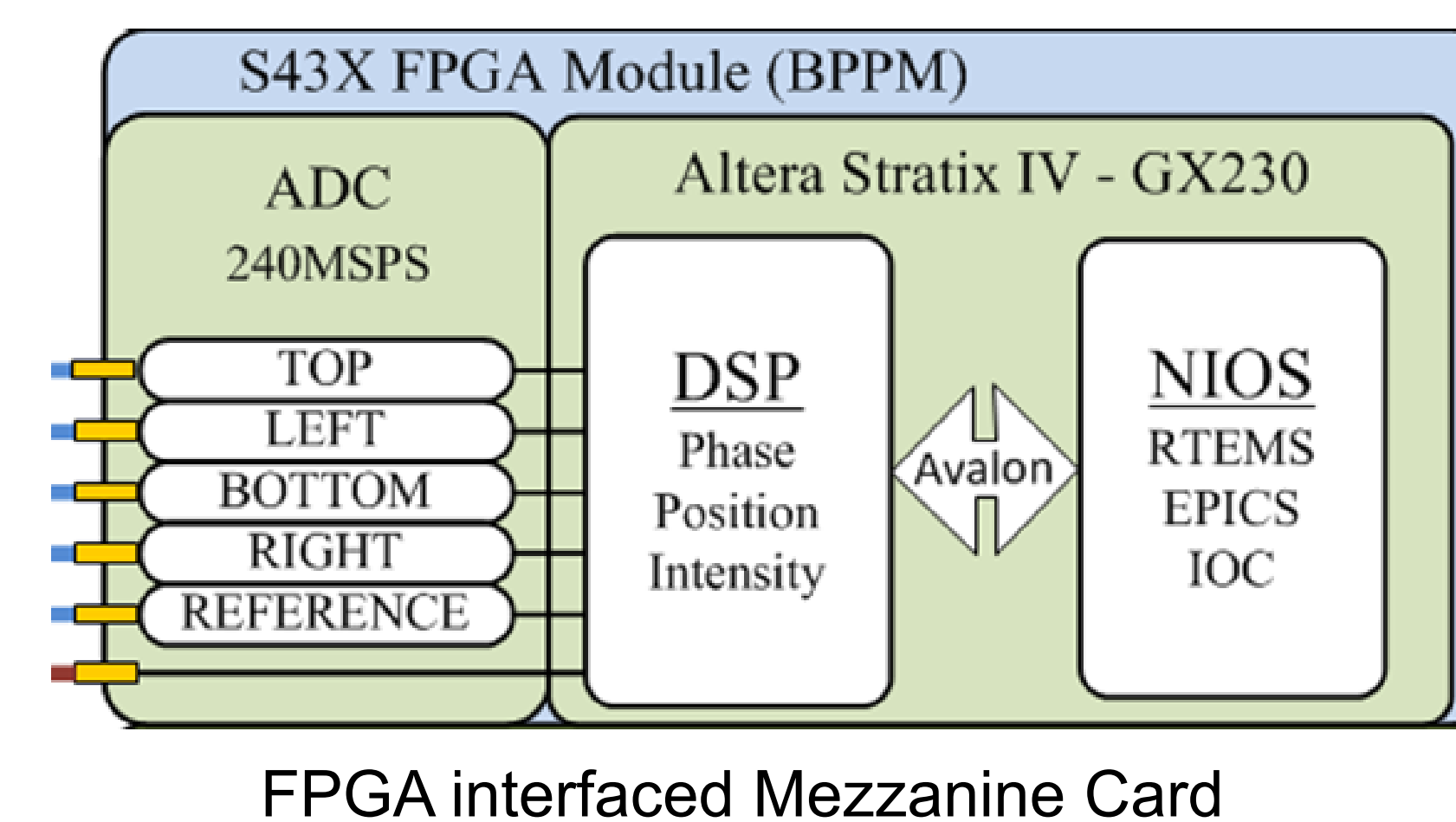
2020
EPICS
cPCI/VPX
cRIO



LANSCE Control System 2020



VPX hardware solution is very adoptable. It consists of a FPGA interfaced Mezzanine Card (FMC), that hosts an Analog Digital Converter (ADC) and an Altera Stratix IV-GX230. The later is hosting an embedded EPICS IOC running the RTEMS operating system on a NIOS-II softcore.



UPGRADE CHALLENGES

- Project focused on engineering solutions that would minimize the number of hardware platforms we would need to introduce
- Funding levels have been flat for the project and did not consider the year to year funding needs to execute the project in the most effective fashion.
- Unexpected funding adjustments for other non-controls project scope elements added a great deal of uncertainty to whether we would be able to do everything we had planned for.
- Therefore, after the design phase we chose to focus the majority of our controls scope elements on the purchase of the equipment vs. purchase & installation.
- Hoping that if we have all the hardware at hand, we find the funding to install it either through remaining project funds, one-time funding, and/or through our maintenance budget.