SIRIUS CONTROL SYSTEM: DESIGN, IMPLEMENTATION STRATEGY AND MEASURED PERFORMANCE

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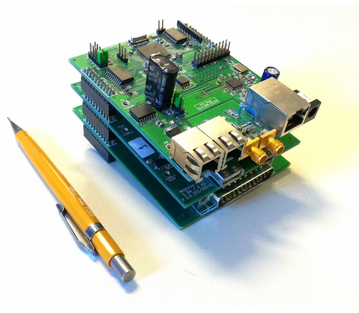
Sirius Control System Highlights

- Designed to be modular, distributted, scalable and cost effective;
- Hardware platform to manage analog and digital I/O and equipment connectivity;
- EPICS compatible;
- Synchronous operations support;

Hardware Implementations



PUC (Universal Control Board)

- CPU board with stacked interface modules;
- ARM Cortex M4 Microcontroller;
- Serial 6 Mbps and Ethernet connectivity;
- First prototype for Sirius Control System;

Analog Modules

- Analog interface modules for equipment control;
- 18 bit ADC and DAC, ±10V operating range;
- Lineartity, repeatability and stability characterization;

Linearity test

DNL	PUC1 DAC		PUC2 DAC		PUC3 DAC	
Range	Min (LSB)	Max (LSB)	Min (LSB)	Max (LSB)	Min (LSB)	Max (LSB)
-9V	-0,235	0,232	-0,165	0,168	-0,396	0,402
-5V	-0,118	0,117	-0,090	0,098	-0,165	0,177
0V	-0,283	0,289	-0,275	0,273	-0,039	0,019
+5V	-0,138	0,138	-0,085	0,085	-0,161	0,170
+9V	-0,193	0,203	-0,156	0,184	-0,295	0,254

Differential non-linearity error measurement for PUC analog outputs.

DNL	PUC1 ADC		PUC2 ADC		PUC3 ADC	
Range	Min (LSB)	Max (LSB)	Min (LSB)	Max (LSB)	Min (LSB)	Max (LSB)
-9V	-0,449	0,481	-0,384	0,311	-0,633	0,560
-5V	-0,279	0,232	-0,397	0,350	-0,318	0,311
0V	-0,240	0,219	-0,279	0,180	-0,161	0,140
+5V	-0,279	0,232	-0,253	0,245	-0,227	0,271
+9V	-0,489	0,389	-0,410	0,376	-0,489	0,547

Differential non-linearity error measurement for PUC analog inputs.

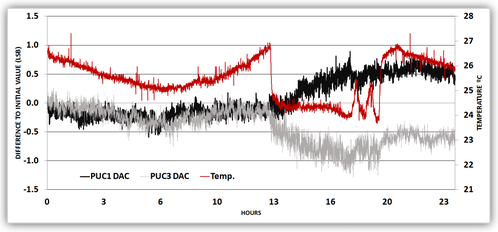
INL	PUC1 DAC		PUC2 DAC		PUC3 DAC	
Range	Min (LSB)	Max (LSB)	Min (LSB)	Max (LSB)	Min (LSB)	Max (LSB)
-9V	-0,096	0,762	-0,280	0,122	-0,717	0,104
-5V	-0,226	0,129	-0,248	0,059	-0,158	0,217
0V	-0,366	0,000	-0,409	0,000	-0,017	0,083
+5V	-0,082	0,257	-0,134	0,157	-0,133	0,263
+9V	-0,224	0,294	-0,304	0,096	-0,249	0,428

Integral non-linearity error measurement for PUC analog outputs.

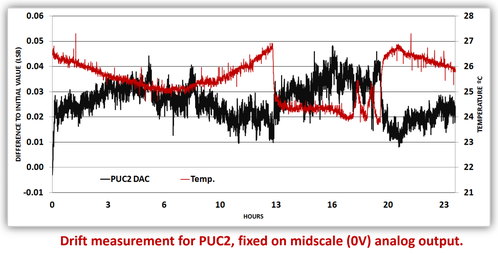
INL	PUC1 ADC		PUC2 ADC		PUC3 ADC	
Range	Min (LSB)	Max (LSB)	Min (LSB)	Max (LSB)	Min (LSB)	Max (LSB)
-9V	-1,067	0,293	-1,102	0,301	-1,824	0,293
-5V	-1,177	0,845	-0,030	1,392	-1,177	0,845
0V	-0,681	0,734	-1,038	0,233	-0,681	0,734
+5V	-0,469	0,875	-1,221	0,174	-0,469	0,875
+9V	-1,520	0,022	-0,224	0,634	-1,520	0,022

Integral non-linearity error measurement for PUC analog inputs.

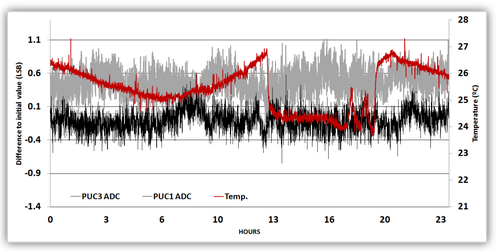
Stability test



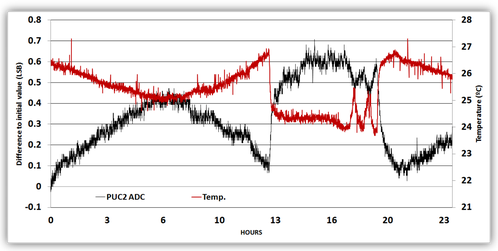
Drift measurement for PUC1 (fixed on -9V) and PUC3 (fixed on +9V) analog outputs.



Drift measurement for PUC2, fixed on midscale (0V) analog output.

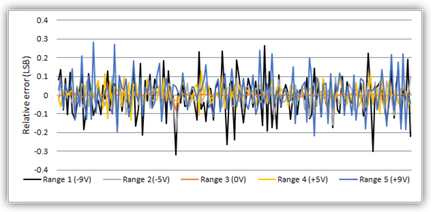


Drift measurement for PUC1 and PUC3 analog input readings.

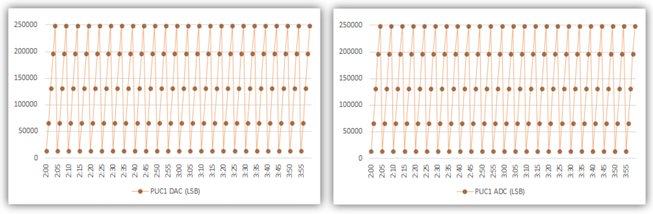


Drift measurement for PUC2 analog input reading.

Repeatability test

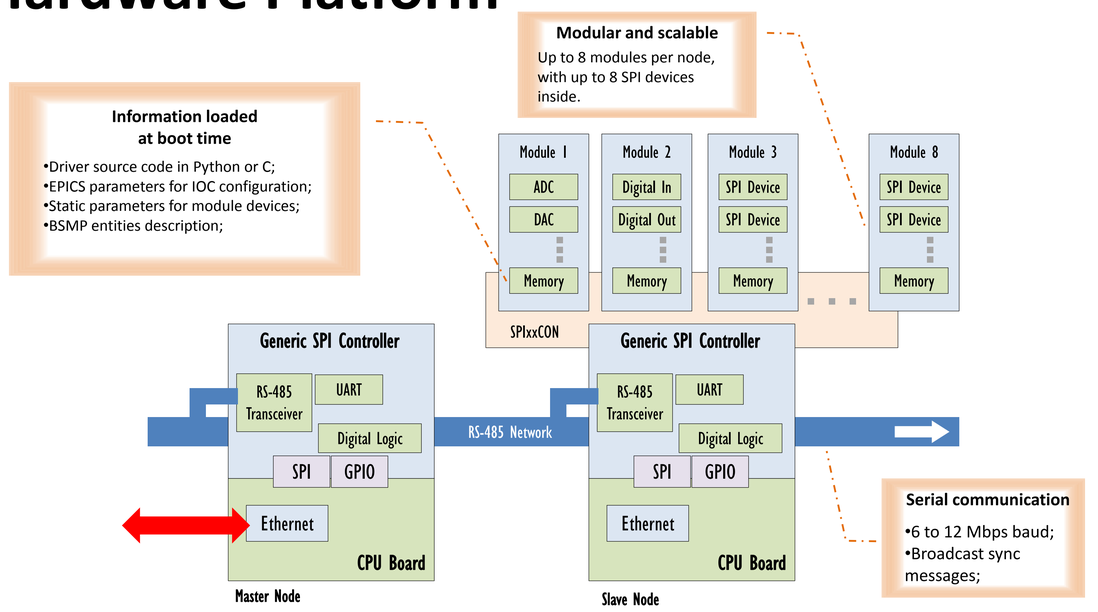


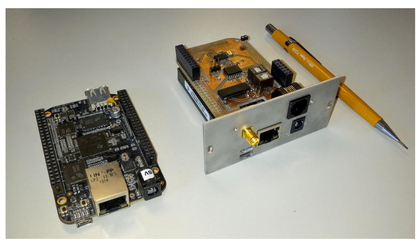
Relative error due to consecutive values in the same range, for PUC1 during repeatability test.



Profile of the repeatability test of PUC1, for analog output and input.

Hardware Platform





Beaglebone Black

- Low-cost open hardware platform;
- Based on ARM Cortex A8, running at 1 GHz;
- Linux-based OS support;
- 2x real-time 32-bit microcontrollers (PRU);
- Ideal for distributted systems;

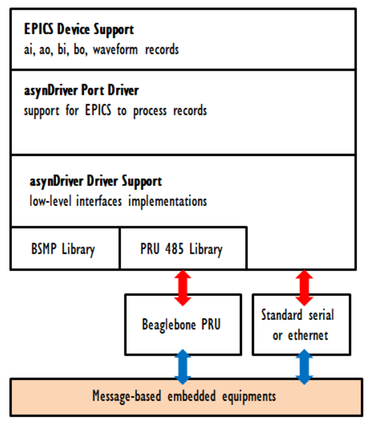
Software Implementations

BSMP (Basic Small Messages Protocol)

- Lightweight protocol for message-based communications;
- Library in C (and Python) with a robust API for implementation;
- Based on configurable entities (variables, groups, curves and functions);

EPICS Device Support

- Based on asynDriver framework;
- Embedded libraries compatible with BSMP and Beaglebone PRU;



PUC EPICS Device Support

Synchronous Support

- Triggers for synchronous operations are transmitted over serial network as broadcast messages;
- Flexible approach, reducing the number of cables from Timing System;

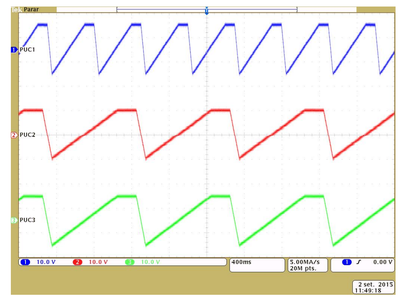
Node	Minimun (us)	Maximum (us)	Average (us)	Std. dev (ns)
PUC 1	13.91	13.99	13.94	17.13
PUC 2	13.94	14.00	13.97	14.54
PUC 3	13.95	14.04	13.98	18.45

Latency of synchronism trigger reception at Beaglebone Black (master) and node (PUC) effective action (after the reception of the broadcast synchronous packet over serial network).

Master	Slave	Minimun (us)	Maximum (us)	Average (us)	Std. dev (us)
PRU	PRU	23.89	23.99	23.94	0.01899
PRU	ARM	179.5	476.5	196.9	16.02
ARM	PRU	379.9	924.6	391.8	22.3
ARM	ARM	1322	6589	1453	387

Latency of synchronism trigger reception at master, and slave node action (after the reception of the broadcast synchronous packet over serial network). Using Beaglebone Black as master and slave, but running software from PRU unit and/or ARM core running Linux.

Selective interruption test: PUC1 attend all the broadcast messages from synchronism, while PUC2 attend only the even ones and PUC3 only the odd ones.



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