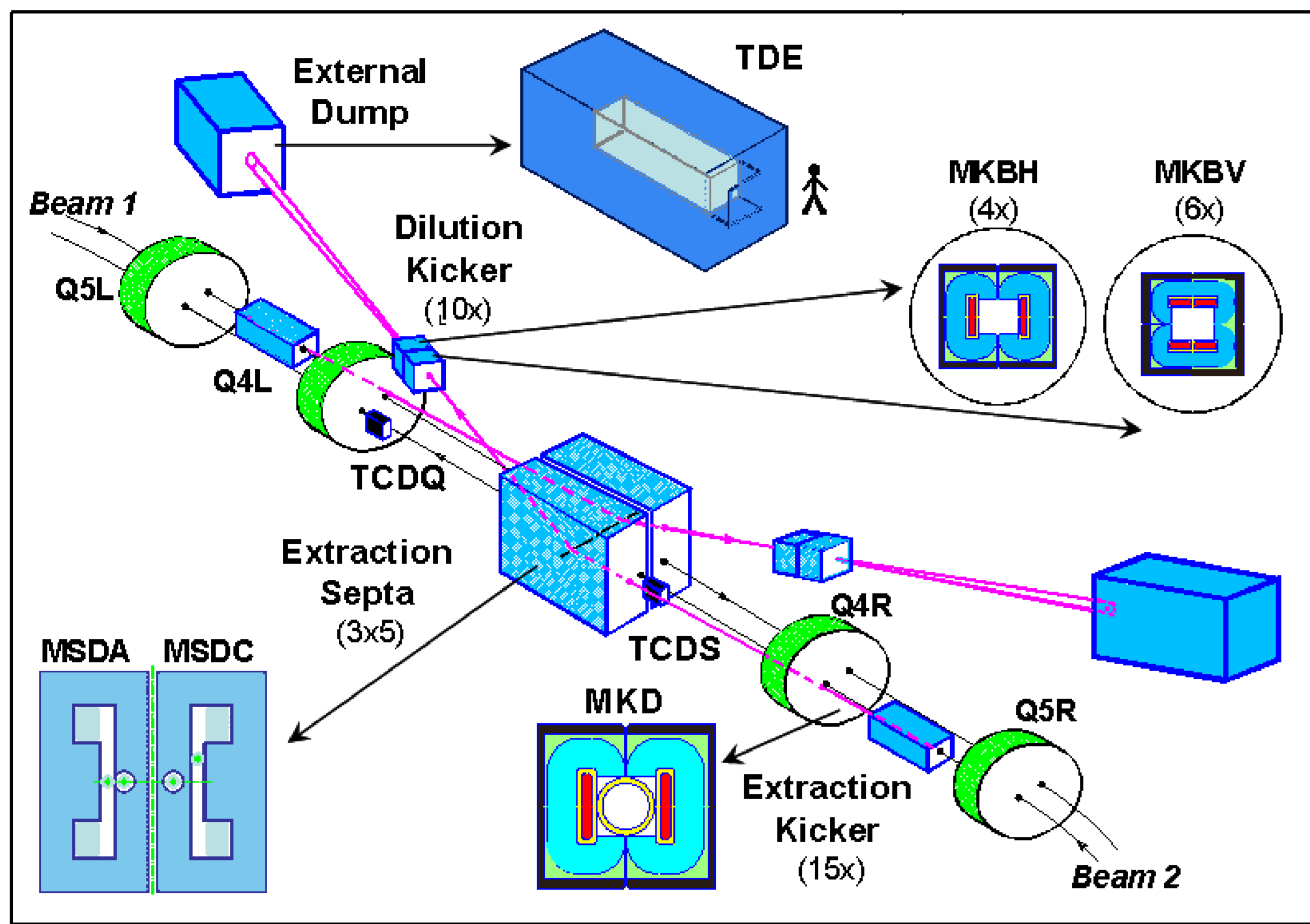
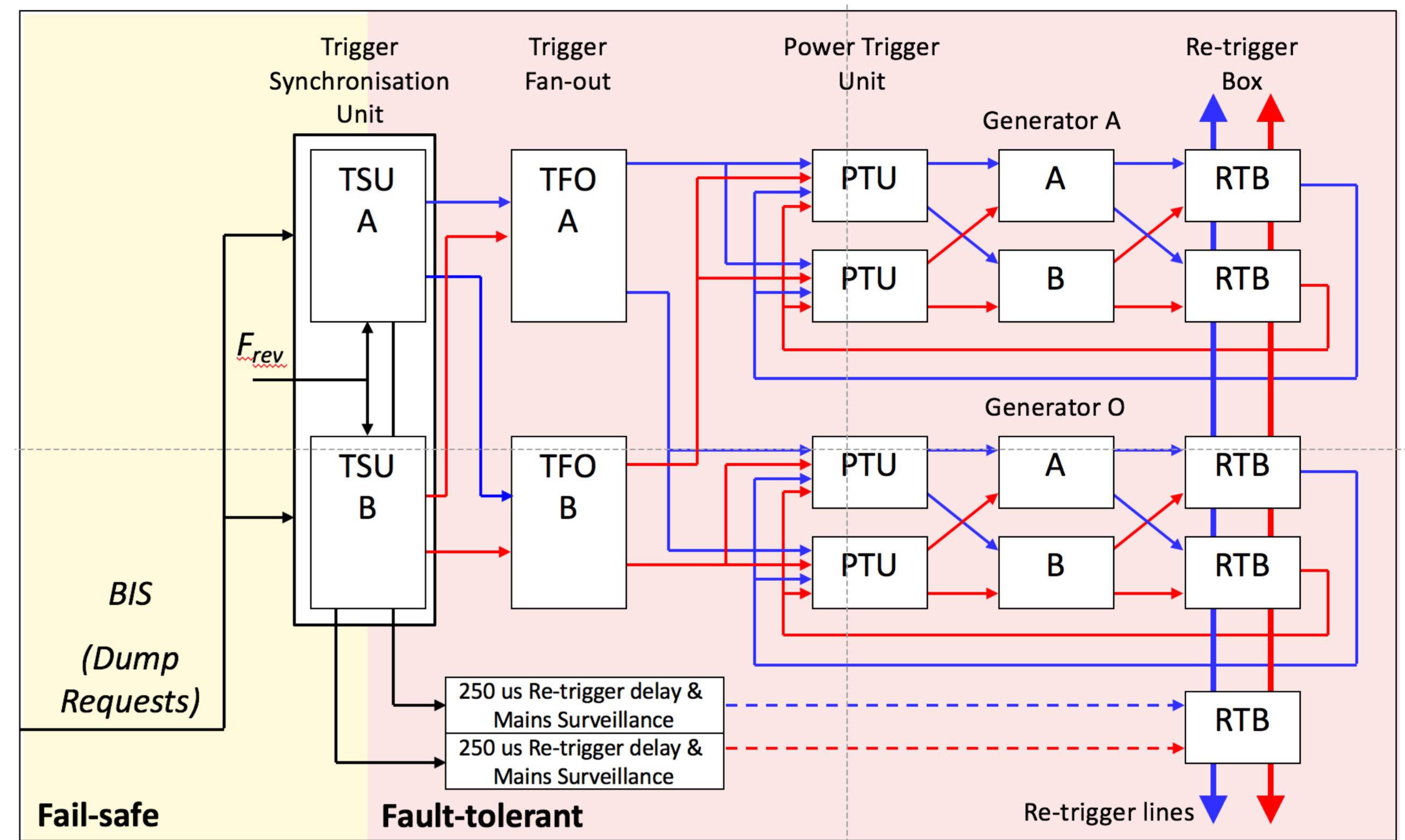


N. Magnin, A. Antoine, E. Carlier, V. Chareyre, S. Gabourin, A. Patsouli, N. Voumard  
CERN, Geneva, Switzerland

## LHC Beam Dumping System



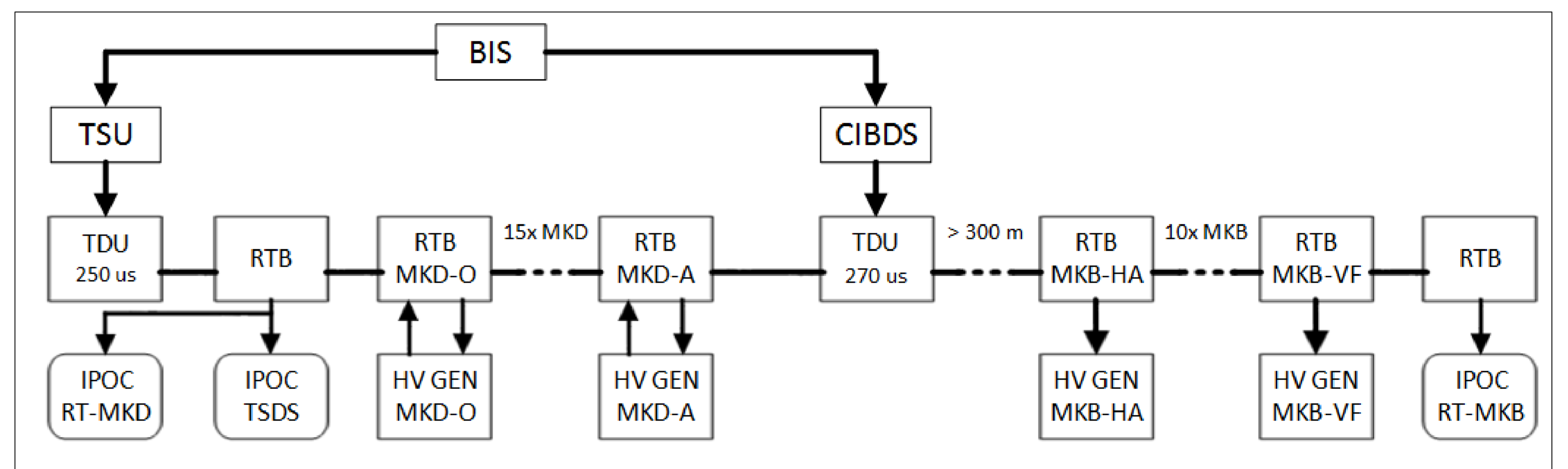
Schematic layout



The LBDS Trigger Synchronisation and Distribution System

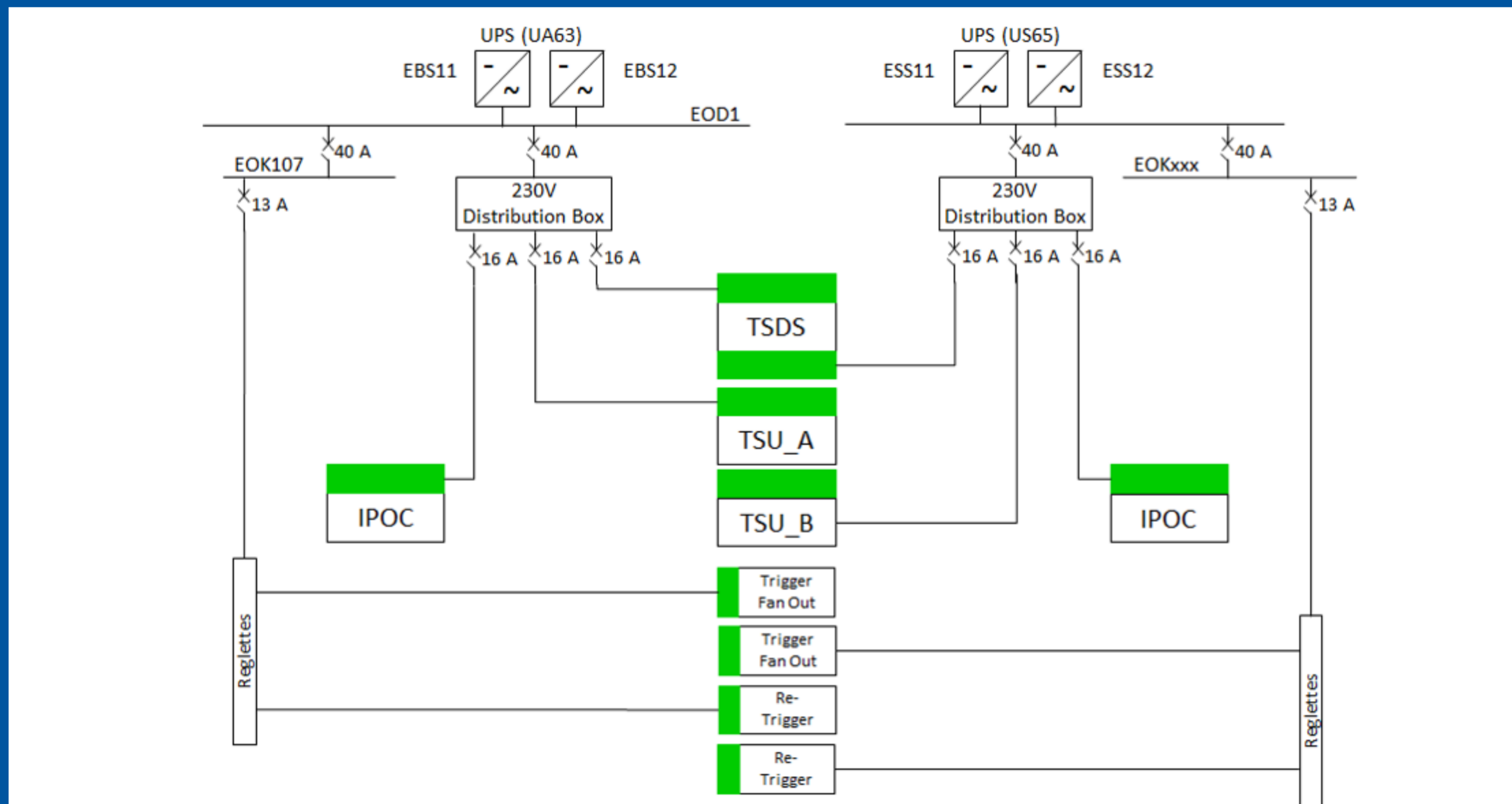
### Re-Trigger System (RTS): Asynchronous triggering of LBDS

- In case of self-trigger of one MKD HVPG (internal pickups in HVPG injects pulses on the RTL)
- To cover the case of synchronous trigger distribution not working, the TSU cards systematically inject a pulse on the RTL through Trigger Delay Units (TDU) with a delay of 250  $\mu$ s w.r.t. the synchronous trigger.



Simplified view of one Re-Trigger Line (RTL)

## Upgrade Power Distribution

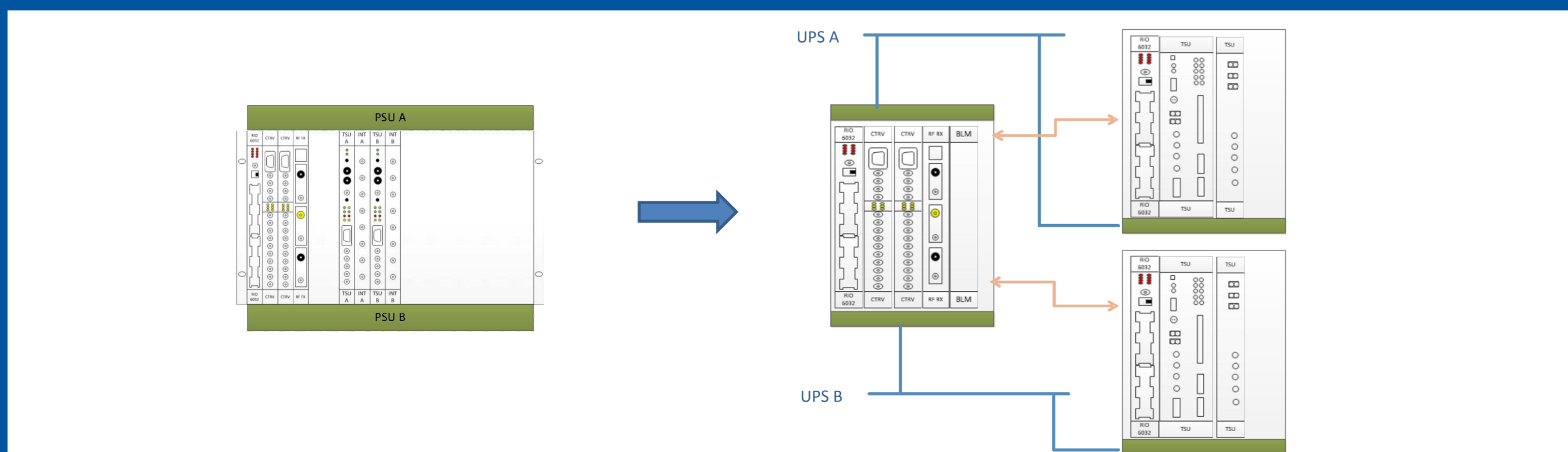


Full redundant electrical distribution

**Motivation:** During LHC Run I in 2012, one computer power supply unit (PSU) failed, causing the loss of one complete UPS.

- Upgrade:**
- Addition of Distribution Boxes, with individual circuit-breaker for each computer PSU;
  - Addition of a second fully redundant UPS for LBDS powering.

## New Deployment of Trigger Synchronisation Unit



New deployment of TSU cards

**Motivation:** During LHC Run I, a new failure mode was identified: In case of failure of the +12V of the VME crate housing the two TSU cards, no dump trigger is issued.

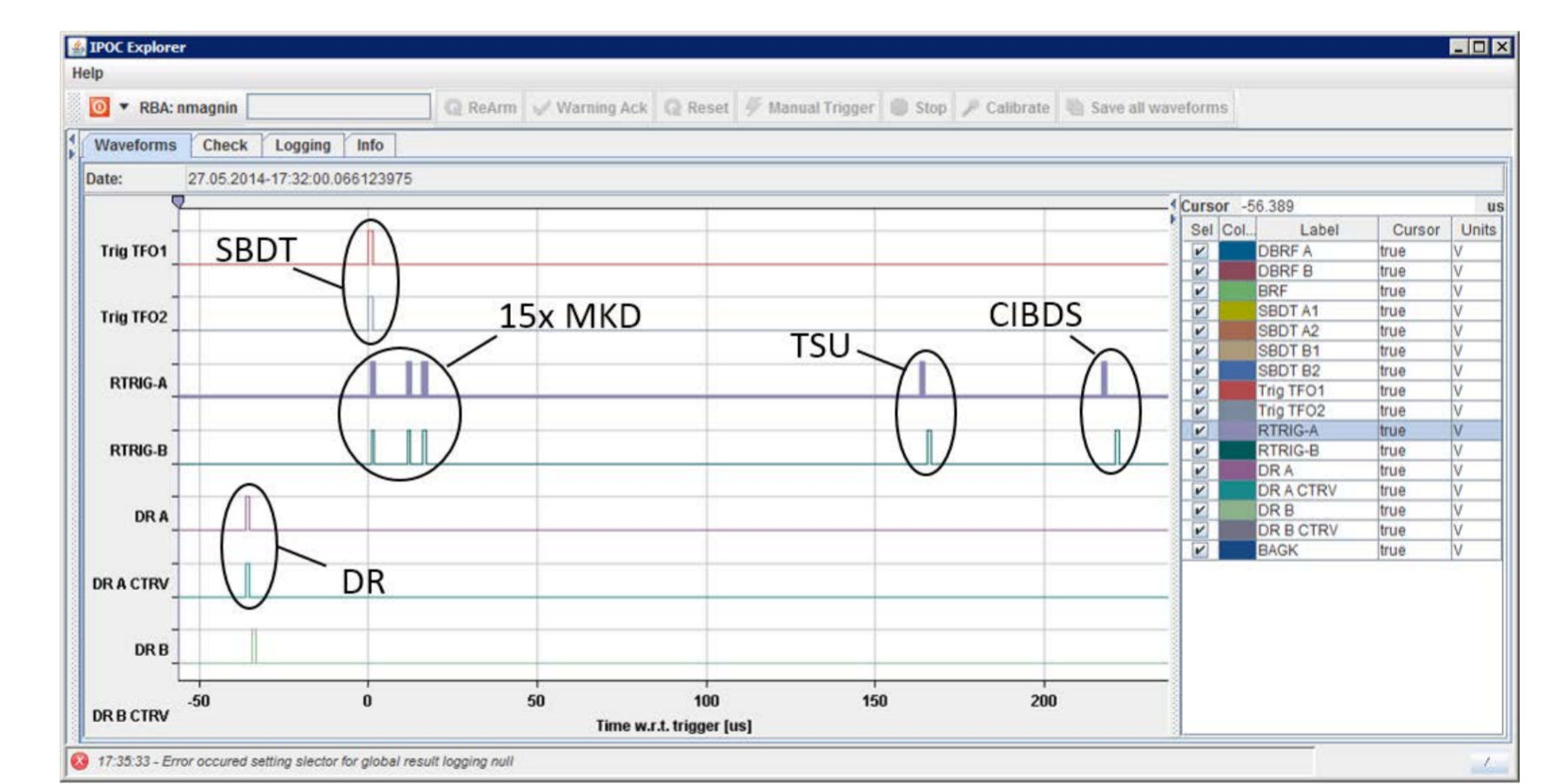
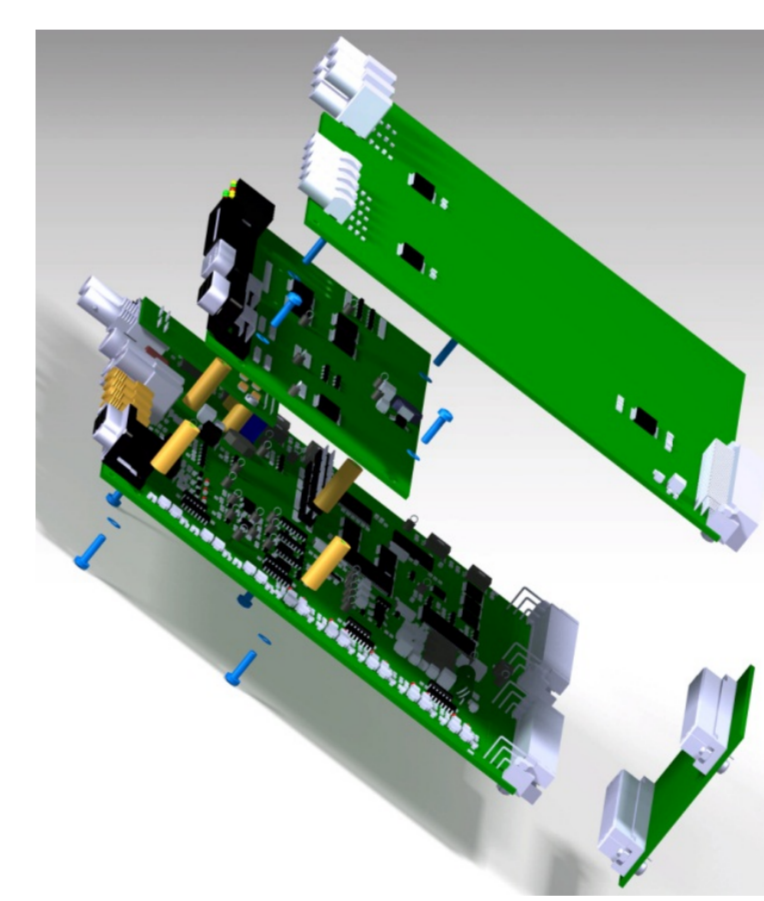
**Upgrade:** The two TSU cards are deployed in individual VME crate, with redundant Power Supply Units.

## Direct Connection From BIS to RTS

**Motivation:** In case of simultaneous failure of both TSU cards, no Dump Request would be executed.

**Upgrade:** A redundant direct link has been established between the BIS and the RTS of the LBDS. A new CIBDS card will inject a pulse on the RTL on a BIS DR through Trigger Delay Units (TDU) of 270  $\mu$ s.

## New Trigger Synchronisation Unit

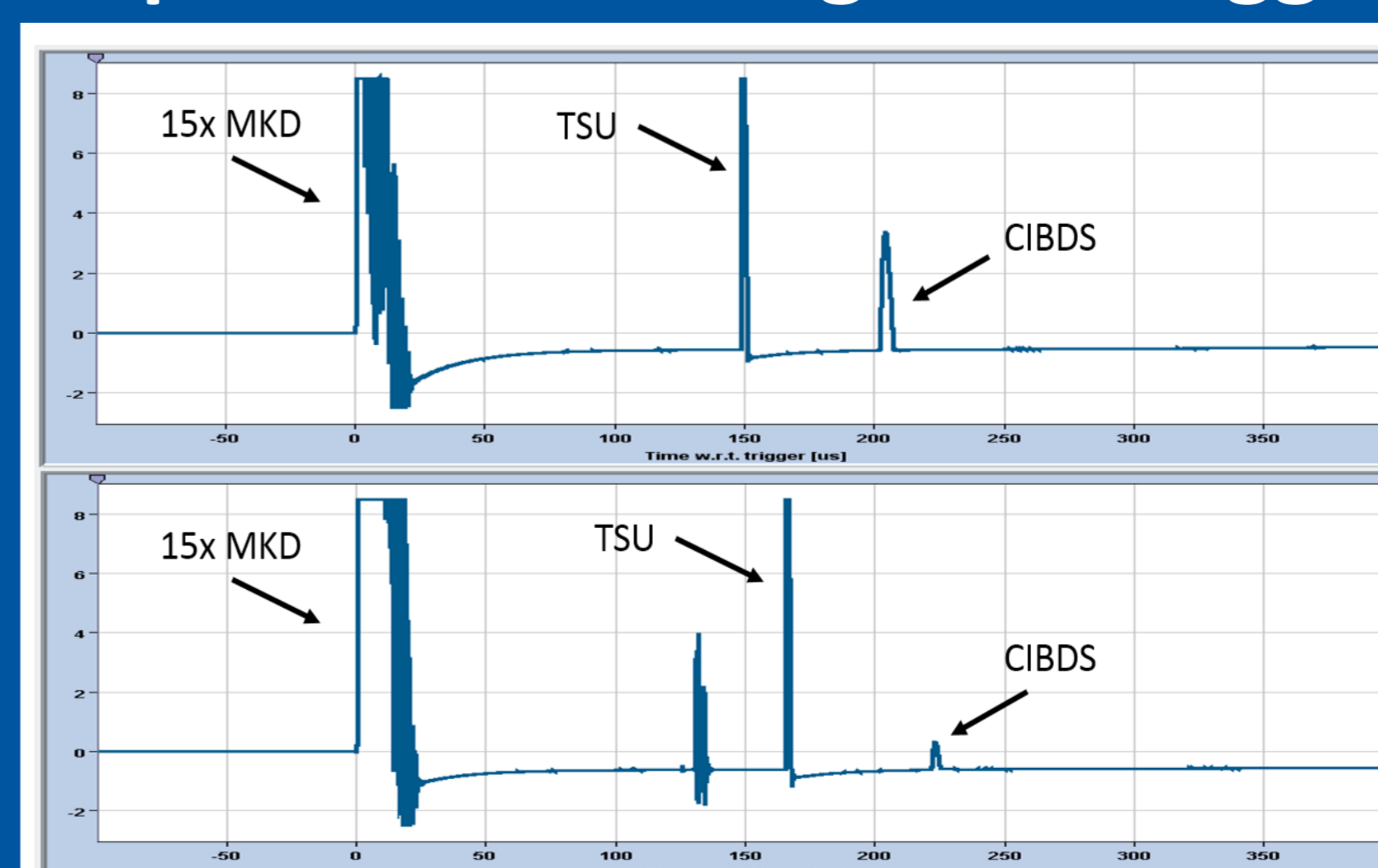


View of some signals captured by IPOC-TSDS

**Motivation:** External review recommendations follow-up.

- Upgrade:**
- Surveillance of all internal voltages (DR is issued to the redundant card in case any power supply failure is detected);
  - Internal surveillance of the CRC of the TSU programmable logic circuits (FPGA). In case of a Single Event Upset corruption a DR is issued to the redundant TSU.

## Improve Monitoring of Re-trigger Lines



View of RTL IPOC signals at 450 GeV and 6.5 TeV.

**Motivation:** Check of re-trigger lines continuity.

- Upgrade:**
- Implementation of an Internal Post Operational Check (IPOC) system at both extremities of the lines;
  - Monitoring of re-trigger lines absorption.