MOM305

Control System for a Dedicated Accelerator for SACLA Wide-Band Beam Line

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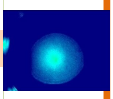
PROJECT

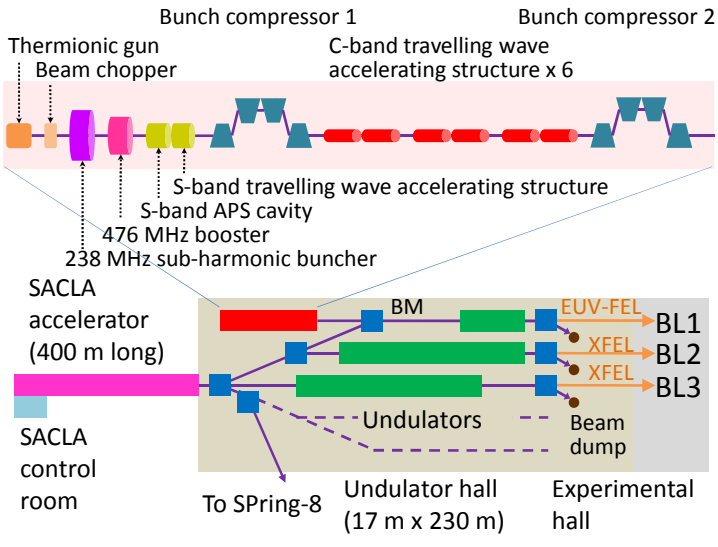
- The X-ray free electron laser facility SACLA in Japan has provided opportunities for the exploration of new science.
- To increase the user experiment opportunity, SCSS prototype accelerator was relocated and modified as a dedicated accelerator for SACLA BL1.
- SCSS prototype accelerator was constructed before SACLA in 2005 and used for EUV-FEL experiment.

Project status

5/2013	SCSS prototype accelerator shutdown	*Done!*
9/2014	Relocation & modification work	*Done!*
7/2015	RF conditioning	*Done!*
9/2015	Beam commissioning start	*Done!*
10/2015	First EUV-FEL observation	*Done!*
3/2016	User experiment at BL1	Will start



THE DEDICATED ACCELERATOR FOR BL1



Design parameters

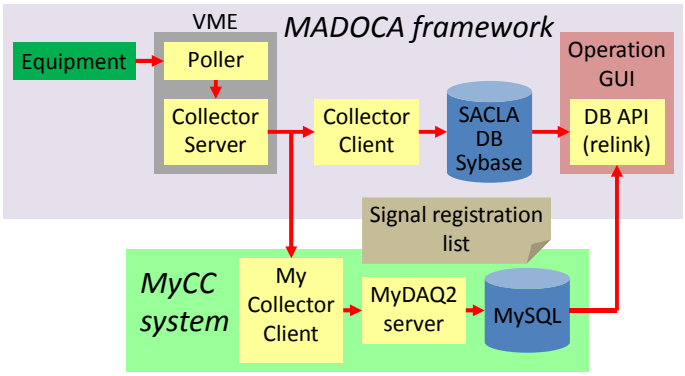
Beam energy	420 MeV	Wavelength	42 nm
Peak current	300 A	Pulse energy	100 uJ
Repetition rate	60 Hz		

CONTROL FRAMEWORK

- MADOCA (Message And Database Oriented Control Architecture) control framework was used.
- We reused all software/hardware resources developed for SACLA.

MyCC

- MyCC, temporary DAQ system compatible with MADOCA, was used at the start of RF conditioning, because some components were not installed yet.
- After the completion of the construction, we transitioned to MADOCA.



- Independent DB (MySQL) from SACLA DB (Sybase)
- No need to change VME processes
- Common signal registration list
- Common function calls between MADOCA DB API and MyCC one

Number of registered signals in SACLA DB

	SACLA	The dedicated accelerator
Analogue data	43,668	2,519
Digital data	16,130	1,103
Total	59,818	3,622

CONTROL HARDWARE

VME system and PLC were mainly used to control equipments.

VME board type and number of boards

CPU	GE XVB601 (Core i7), Sanritz SVA041 Pentium M)	24
High speed A/D	MELOS MVD-ADC01 (238 MHz sampling, 16 bit resolution, and 4 channels input)	28
High speed D/A	MELOS MVD-DAC02 (238 MHz sampling, 16 bit resolution, and 4 channels output)	6
High resolution A/D	MELOS MVD-DAC04 (1 MHz sampling, 24 bit resolution and 4 channels input)	1
Trigger delay	MELOS TDU (32 bit delay, 4.2ns/bit, jitter 0.9 ps, 8ch output)	7
Optical remote I/O	Hitz OPT-VME/OPT-DIO (for magnet PS)	15
PLC interface	Hitz, FL-net board	13
Interrupt register	ARKUS Axvme4900	3