STATUS DEVELOPMENT OF SIRIUS TIMING SYSTEM

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Abstract

Sirius is a new low-emittance 3 GeV synchrotron light source under construction in Brazil by LNLS, scheduled for commissioning in 2018. Its timing system will be responsible for providing low jitter synchronized signals for the beam injection process as well as reference clocks and triggers for diverse subsystems such as electron BPMs, fast orbit feedback and beamlines distributed around the 518 meters circumference of the storage ring, Booster and Linac. It will be composed of Ethernet-configured standalone event generators and event receivers modules developed by SINAP through a collaboration with LNLS. The modules will be controlled by remote EPICS soft IOCs. This paper presents the system structure and the status of the development, some options for integrating it to the Sirius BPM MicroTCA platform are also discussed.

INTRODUCTION

Sirius light source consists of a 150 MeV Linac, a 150 MeV to 3 GeV booster synchrotron and a 3 GeV, 518 meters circumference, storage ring with 20 straight sections, achieving a very low beam emittance of 0.24 nm·rad [1]. Many devices must be triggered synchronously by a low jitter timing system to guide the electrons from the Linac to the storage ring.

The main purpose of a timing system is to generate and distribute deterministic signals to control the beam injection process. Secondary purposes are to provide timestamps for diverse subsystems to ensure a time-coherent behaviour of data acquisition and to deliver reference clock for the electron BPM and fast orbit feedback systems.

The range of possibilities considered to perform the Sirius timing system can be summarized in four major approaches: (i) a completely commercial timing system [2], (ii) a solution entirely based on scientific test and measurement instruments [3], (iii) an in-house development and (iv) collaborative options, such as White Rabbit Project [4] and SINAP timing system [5]. After surveying these possibilities, the SINAP timing system was chosen based on the available functionality it could offer, proven reliability [6] and collaboration opportunity.

REQUIREMENTS

The Sirius injection system operates with a 2 Hz repetition rate, which must be synchronized to the mains at 60 Hz to turn repetitive the ripple effect of the power supplies on the injected beam in the accelerators. Trigger signals should be derived from the RF frequency to synchronize pulsed elements on Linac, Booster and storage ring to electron bunches. The 90 keV e-gun, that will operate in single-bunch and multi-bunch modes, is the pulsed element with the most demanding trigger signal, requiring jitter less than 50 ps rms, coarse delay resolution of 2 ns and fine delay resolution of 20 ps.

After the commissioning phase, top-up is foreseen to be the Sirius normal operation mode, in which a bunch current measurement system to take the bunch current profile may be necessary to perform the bunch selection. Hence, Sirius timing system should support injection to any bunch and software integration to external systems. Furthermore, other requirements include that critical signals needs to be transmitted through optical fibres to minimize EMI, electrical outputs requires TTL level compatibility and inputs for external triggers are essential.

Table 1 presents the main parameters about Sirius and timing system specifications.

Table 1: Main Sirius Parameters and Timing Specifications

Parameter	**Value**
RF freq. (Storage Ring & Booster)	499.658 MHz
Storage ring circumference	518.4 m
Storage ring harmonic number	864
Storage ring revolution freq.	0.578 MHz
Booster circumference	496.8 m
Booster harmonic number	828
Booster revolution freq.	0.603 MHz
Coincidence number	19872
Coincidence frequency	25.144 kHz
Linac RF frequency	2.997 GHz
Repetition rate	2 Hz
Specification	**Value**
E-gun rms jitter	< 50 ps
E-gun trigger coarse delay step	2 ns
E-gun trigger fine delay step	20 ps
General trigger delay step	8 ns
Electrical outputs	TTL level
Event clock freq. ($\frac{RF\ freq.}{4}$)	124.915 MHz

SYSTEM DESIGN

Sirius timing system is event-based [7], i.e. an event generator (EVG) broadcasts event frames to event receivers (EVR and EVE) through a star topology optical fibre network. An event frame consists of an 8-bit event code and an 8-bit distributed data bus. Each decoded event can generate configurable output triggers and each bit of the distributed data bus maps a channel clock, which can be configured to any integer sub multiple of the event clock. Since the event clock is derived from the RF frequency, this and the channel clocks are synchronized. Therefore, an event

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receiver can output configurable triggers and synchronized clock signals to several devices in the accelerators. During an injection process, a sequence of event frames is transmitted every 500 ms (repetition rate).

The event receivers differ according to the output type. While EVEs have LVTTL electrical outputs, EVRs have polymer optical fibre and glass optical fibre outputs. The output signals from EVRs are converted to electrical TTL level by the optical to electrical converter modules STD-SOEs and SOEs, in case of polymer fibre, or STD-MOEs, in case of glass fibre. STD-MOEs and STD-SOEs modules are standalone 19 inches 1U boxes with four optical to electrical converter channels, while SOEs are small boxes with only one channel (Fig. 1).

Figure 1: Optical to electrical converters STD-MOE, STD-SOE and SOE.

EVG, EVR and EVE are also 1U boxes and are configurable through Ethernet UDP interface. All modules were jointly specified by LNLS and SINAP and have isolated electrical inputs for interlock purposes. The development and construction were carried out by SINAP. System modules, fibres and cables are listed in Table 2. A diagram of Sirius timing system network and modules involved in the injection process is shown in Fig. 2.

Table 2: System Modules, Fibres and Cables

Module	**Quantity**
EVG	1
EVR	5
EVE	3
STD-MOE	5
STD-SOE	3
SOE	12
MicroTCA timing board	20
Fibre & Cable	**Quantity**
Level-1 glass fibre (250 m)	8
Level-2 glass fibre (150 m)	13
Level-3 glass fibre (150 m)	20
Polymer fibre (50 m)	20
Electrical cable (20 cm)	35

Hardware

The EVG issues event codes and data clocks at the rate of the event clock, where the events are read at the same rate from a block of RAM, writeable through the Ethernet

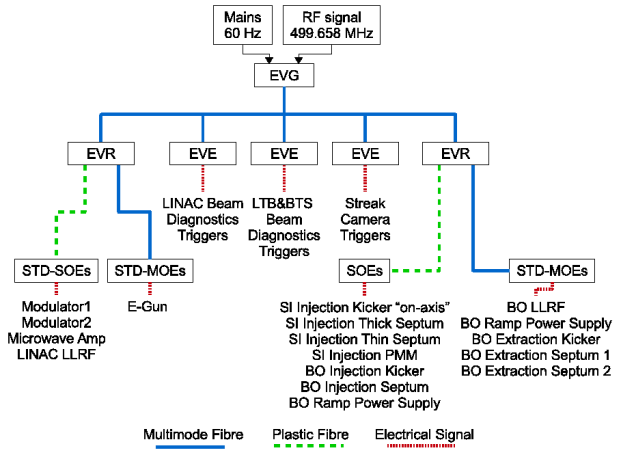

Figure 2: Diagram of Sirius timing system concerning injection process.

UDP interface, used to store a sequence of events. The 2 Hz repetition rate results from the AC line (mains 60 Hz) divided by 30 and it is internally synchronized to the coincidence frequency. On the EVG front panel there are two electrical inputs, one to the RF signal and another to AC line as well as 8 multimode glass optical fibre transceivers to downstream modules.

In the EVR, each output trigger can be configured to be routed to one of the 12 multimode polymer optical fibre outputs on the rear panel or to one of the 8 multimode glass optical fibre outputs on the front panel. The pulse width for each output is adjustable with a resolution of one event clock period (~8 ns). Programmable delays are also available on the front panel outputs, with coarse and fine resolutions of 1/20 event clock period (~0.4 ns) and 5 ps, and on the rear panel outputs with a resolution of one event clock period. Clocks from distributed data bus can be output only on the front panel. Due to the fine delay adjustment of EVR, it is possible to target any bunch by delaying the e-gun trigger with the 1/20 event clock period resolution and other devices with at least one event clock period resolution.

The EVE has 8 electrical outputs mapping decoded clocks or events. Each decoded event generates a configurable output trigger with coarse and fine delay resolutions of 1/20 event clock period and 5 ps, and adjustable pulse width with one event clock period resolution. Another output on the front panel provides a recovered clock derived from the event clock multiplied by 1, 2, 4, 5 or 10, synchronized to the RF.

Distribution Network

The timing distribution network is based on OM3 multimode glass optical fibre operating at 2.5 Gbps rate for distances over 250 meters and multimode polymer optical fibre over distances up to 50 meters. In order to minimize the effect of thermal drifts over the optical links, the length of the fibres is equal on each level.

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Software

The timing system software runs an EPICS base-3.14.12.4 IOC on a Linux environment. The IOC is structured in two parts, low and high levels.

The low level implements UDP communication interface, hardware diagnostic and control, i.e. UDP data frames are used to read and write registers that configure and monitor parameters of the modules, such as prescalers of the distributed data bus on the EVG or widths and delays of the EVR outputs.

The high level part controls the injection process by managing the fill pattern, bunch selection and interface with bunch current measurement system to implement the top-up injection mode. Furthermore, it also implements an abstraction layer that converts prescalers into time units and maps the timing system hardware outputs to the connected devices, providing process variables to configure their triggers.

Operator interface panels were developed using CSS (Control System Studio) to monitor and operate the timing system.

Developments

Once the Sirius timing system is able to deliver trigger and clock signals synchronized to the RF, these signals can be used by diverse subsystems, such as electron BPMs, fast orbit feedback and beamlines, to provide reference clocks, perform synchronized actions or timestamps to ensure coherence of acquired data.

Since electron BPM electronics and fast orbit feedback systems adopted the MicroTCA.4 standard [8], a fully compliant timing receiver board is under development by LNLS to distribute triggers and reference clocks for those electronics. A conceptual prototype of a MCH clock distribution board is shown in Fig. 3. Similar approaches with different form factors have been studied to attend beamline demands.

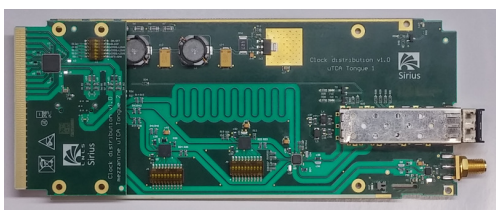

Figure 3: Prototype of the MicroTCA clock distribuition board developed by LNLS.

An important point concerning coherence of acquired data is the post mortem event distribution. For Sirius, this event will be broadcasted over the timing system network to request all relevant devices to store the last buffered measurements. Thanks to the deterministic transmission of the post mortem event, buffers can be precisely time-aligned. This feature will be achieved by a few hardware and FPGA firmware modifications of the EVG, allowing it to receive electrical triggers. A simplified diagram representing part of the timing system network responsible for distributing the signals described in this section is shown in Fig. 4.

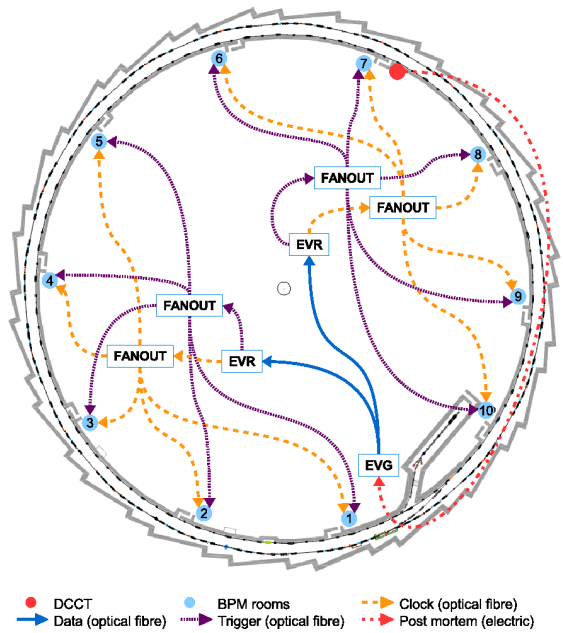

Figure 4: Simplified diagram of Sirius timing system concerning triggers and reference clocks distribution.

TEST RESULTS

The performance achieved by SINAP modules [5] for short-term and long-term (24 hours) jitter between output triggers and the RF master clock were confirmed in tests carried out by LNLS. All modules were verified and typical results indicate short-term jitter values less than 10 ps rms and long-term jitter around 20 ps rms (Fig. 5). These tests were performed using a Rohde & Schwarz SMA100A signal generator and an Agilent DCA-X 86100D 20 GHz bandwidth oscilloscope.

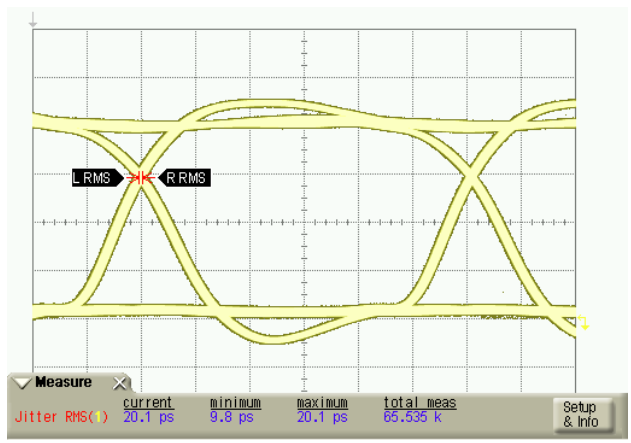

Figure 5: EVE long-term (24 hours) jitter test result.

The short-term jitter of our MicroTCA timing board was characterized using a Rohde & Schwarz FSUP signal source

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analyzer (Fig. 6). The main purpose was to identify not only the rms jitter, but also the phase noise components of the reference clock signal to source the ADCs of the electron BPM electronics and, for this reason, a particularly relevant bandwidth (1 Hz to 5 MHz) was selected. The measurement is shown in Fig. 7, where the rms jitter is less than 5 ps.

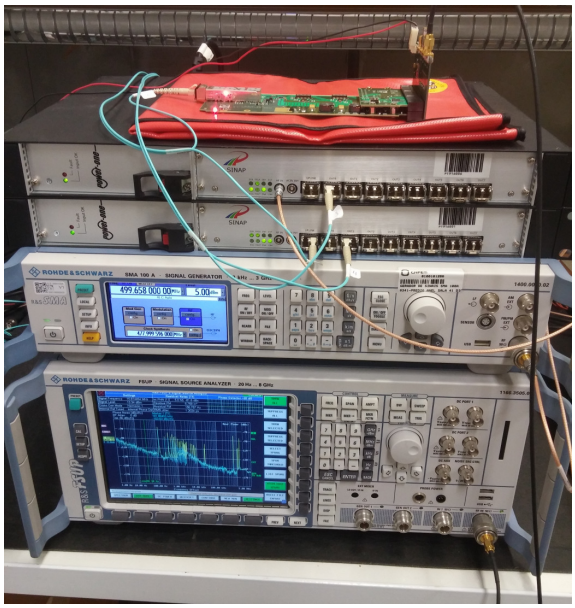

Figure 6: Test setup of MicroTCA timing board. Up to down: MCH board, EVG, EVR, signal generator and signal analyzer.

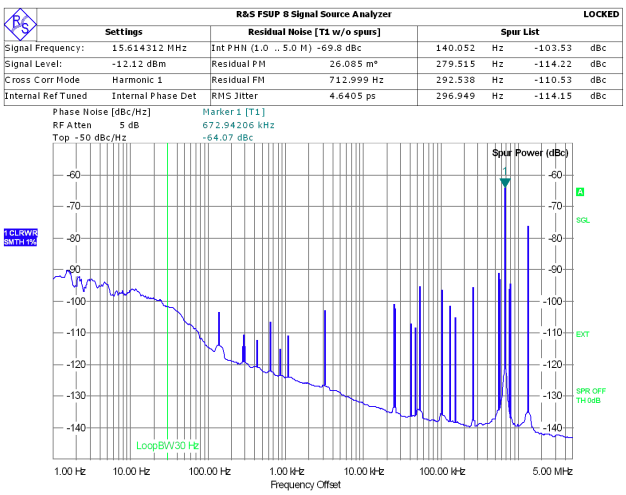

Figure 7: Phase noise analysis of MicroTCA clock distribution board.

CONCLUSIONS

The Sirius timing system structure and functionality necessary to operate during the commissioning phase are completely defined, specifications were achieved and the system has flexibility to accommodate the future developments. Benchmark tests will be performed to characterize propagation delay of optical fibres and to validate the reduced impact of thermal drifts among fibres with the same length. The first units of the MicroTCA timing boards will be produced at the beginning of the next year.

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