OPERATION STATUS OF J-PARC TIMING SYSTEM AND FUTURE PLAN

N. Kamikubota#, N. Kikuzawa, F.Tamura, and N. Yamamoto
J-PARC-Center, KEK & JAEA, Tokami-mura, Ibaraki, Japan

Abstract

The beam commissioning of J-PARC started in 2006. Since then, the timing system of J-PARC has contributed stable beam operation of accelerators. The present timing system is reviewed from the aspects of history, fiber-optic cable network, VME modules and their configurations, followed by upgrade studies for the future.

INTRODUCTION

J-PARC (Japan Proton Accelerator Research Complex) is a high-intensity proton accelerator complex, located in Ibaraki, Japan. It consists of three accelerators: a) 400-MeV linac (LI), b) 3-GeV Rapid Cycling Synchrotron (RCS), and 30-GeV Main Ring (MR), and three experimental facilities: d) Material and Life Science Experimental Facility (MLF), e) Neutrino Experimental Facility (NU), and f) Hadron Experimental Facility (HD) [1-3].

In J-PARC, there are two time cycles. The rapid cycle, 25 Hz, is used at LI, RCS and MLF. Through LI was designed to be operated at the 50-Hz repetition rate, current operation is 25 Hz. The slow cycle is used at MR, NU and HD. In 2015, when MR delivers proton beams to NU (HD), 2.48s (6.00s†) is used, respectively. Since the slow cycle determines the overall time behaviour of accelerators, it is often called "machine cycle". Two different cycles are co-exist in J-PARC.

The J-PARC Timing System started operation since 2006. The purpose is to provide a trigger to each of the accelerator components with a specified delay. In general, only one trigger is necessary within the 40ms (2.48s/6.00s) time slot for the rapid-cycle (slow-cycle) machines, respectively.

PRESENT TIMING SYSTEM

History and Overview

The early studies for the J-PARC controls were carried out in 2003 [4], in which the design for the timing system was one of the issues. In 2003, the VME-bus modules for timing control, both the send module and the receiver module were developed in collaboration with domestic companies [5]. Mass productions of VME modules and related NIM modules were in 2005-2007. The first beam to the LI (RCS, MR) was in 2006 (2007, 2008), respectively. Summarized history is shown in Figure 1.

#norihiko.kamikubota@kek.jp
† 5.52s after RUN64, October 2015

The control system for the J-PARC, including the timing system, is based on EPICS toolkit [6]. Both low-level support (device driver and EPICS databases) and high-level applications for the timing system were developed by ourselves. In order to manage table-formatted registers of VME modules, the waveform record-type of EPICS is used. Java and Python have been preferred for high-level GUI applications. .

In 2015, we have 118 (43, 45) receiver modules, which correspond to ~540 (~220, ~300) end-point signals for LI (RCS, MR), respectively. In addition, a few receiver modules exist for each of three experimental facilities. Only one send module exists for the whole accelerator complex.

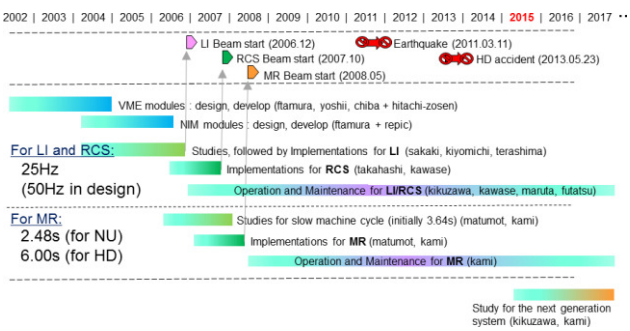

Figure 1: History of the J-PARC timing system.

Base-signals and Their Distribution

We have three "base-signals": a) 12MHz master clock (CLK), b) 25Hz trigger (Trig), and c) type-code (Type). The CLK is provided by a commercial high-stability function generator. The Trig is generated from the master clock, and used as the start signal of each rapid-cycle. The Type, a 32-bit number, is sent at the Trig rate after serialized. A receiver module uses it to generate delayed trigger signals during the next rapid-cycle.

We have fiber-optic cable networks throughout our facility buildings. Three base-signals are generated in the Central Control Building (CCB), then distributed to all the facility buildings using the fiber network (Figure 2).

A schematic view of base-signal distribution is shown in Figure 3. Several E/O, O/E and fan-out modules are used. All of the receiver modules in facility buildings receive the same base-signals.

ISBN 978-3-95450-148-9

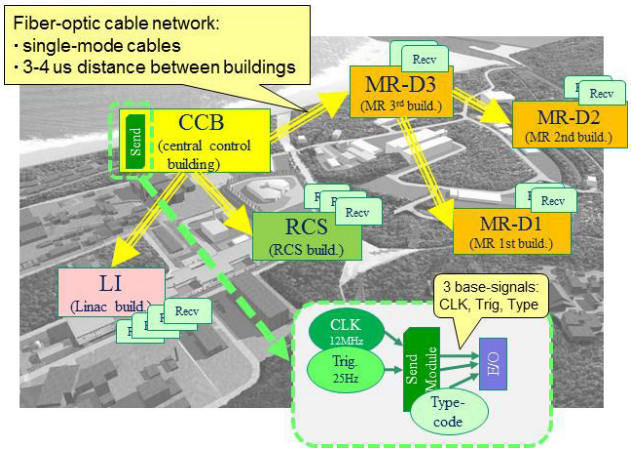

Figure 2: Fiber-optic cable network and the base-signals.

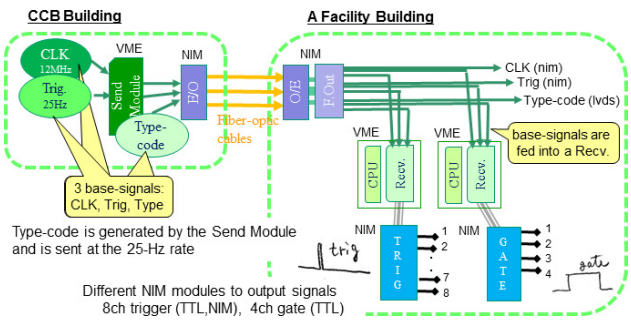

Figure 3: Schematic view of the base-signal distribution.

Send Module

The core of the J-PARC timing system is the send module. It has a type-memory, which consists of 64 type-sequences. At a run-time, one type-sequence is selected and used. The send module sends a type-code in the selected type-sequence one-by-one at the 25-Hz rate. The length of the type-sequence corresponds to the machine cycle; for example 62 (150) type-codes turn to the 2.48s (6.00s). The maximum size of a type-sequence is 1024.

A type-code is a 32-bit number, divided into four subsections: M1 (7bit for spare), M2 (8bit for LI), M3 (8bit for RCS) and M4 (8bit for MR). Each receiver module is set to use one of the subsections, thus only 8-bit is used at a run-time. The MSB (the 31st bit) is used to notify the end of the type-sequence.

Figure 4 is a GUI screen for the send module control in edit mode. Type-sequences and type-codes used in our operations are shown. In Figure 4. The red area is the MR injection period. Values of M2 (for LI) and M3 (for RCS) are different. LI and RCS behave differently during the MR injection according to the received type-codes.

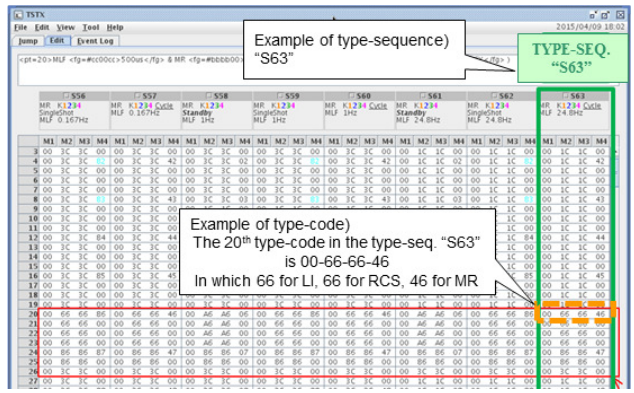

Figure 4: Java-based GUI for a send module control.

Receiver Module

A receiver module is capable to control eight independent delays, with the time resolution of 10.41ns. NIM modules are used to generate pulsed or gated signals (Figure 3). A receiver module has a LUT (Look-up-Table), which contains 256 x 8 delay-words. One delay-word determines the behaviour of one of eight channels, according to the received type-code.

A delay-word contains 24-bit delay count and control bits. After receiving a 25-Hz trigger, an internal counter is reset and starts up counting at the 96 MHz rate. When the counter reached at the delay count in the delay-word, an output trigger is generated. The MSB (the 31st bit) is used to disable output. The internal 96-MHz clock is produced from the 12-MHz master clock by a PLL.

A special control bit, the 30th, is used to continue counting even when the next 25-Hz trigger arrived. This feature is used to generate a large delayed signal, which exceeds the rapid-cycle (40ms). The maximum possible delay is about 170ms.

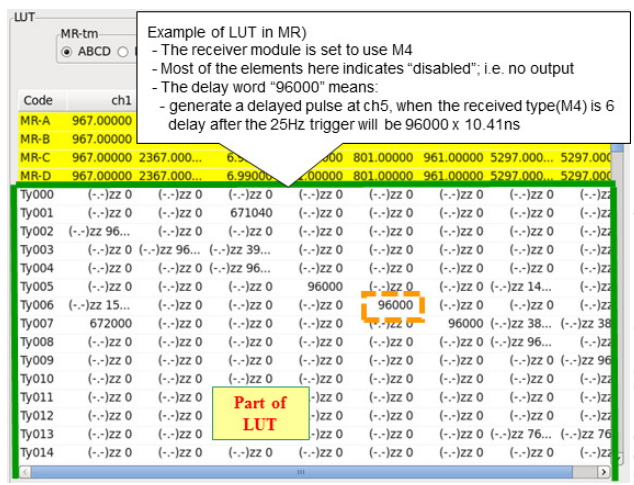

Figure 5: Python-based GUI for a receiver module control.

ISBN 978-3-95450-148-9

Figure 5 shows a part of LUT of a receiver module in MR. Most of elements in the LUT indicate "disabled", using the MSB. The highlighted number "96000" means: 1) the ch5 will generate a delayed output when the received type-code (M4 subsection) is 6, 2) amount of delay will be 96000 x 10.41ns after the 25-Hz trigger.

OPERATION AND EXPERIENCES

Beam-slot Sequence in Single Machine Cycle

Each of the 25-Hz time slots in single machine cycle has a predefined beam destination, which we call "beam slot". In 2015, typical operation modes for beam delivery to experimental facilities are: (a) MLF and NU with the machine cycle 2.48s, and (b) MLF and HD with the machine cycle 6.00s. Assignments of beam slots are shown in Figure 6.

In both operation modes, 4 beam slots, from 20th to 23rd, are assigned for MR injection, followed by 2 empty slots. Empty slots are needed to avoid miss-steering caused by the residual magnetic field of the switching magnet. New small magnet to compensate the residual field is in test [7].

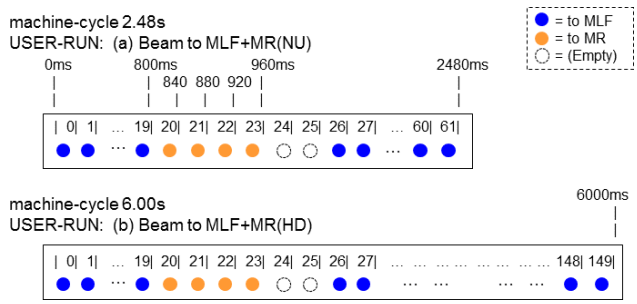

Figure 6: Typical beam-slot sequences.

Transitions of Beam-slot Sequences

In real machine operation, many beam-slot sequences are needed, and transitions between sequences must be considered. In the J-PARC timing system, switching a type-sequence in the send module to another results in a sequence transition. In Figure 7, upper sequences are for beam deliveries to experimental facilities, and lower for single-shot machine studies. Variety of transitions are possible using 64 type-sequences in the send module. Independent beam start and stop for MLF and MR, which is inevitable for our operation, is realized by this feature of the send module.

In daily operation, an accelerator operator changes beam-slot sequences manually. However, when a MPS event (machine fault) occurs, the sequence is changed automatically to the stand-by mode.

Change of the MR operation mode between NU and HD is once per a few months. This is carried out by a change of the machine cycle, left to/from right as shown in Figure 7. The change procedure is done manually also by an operator.

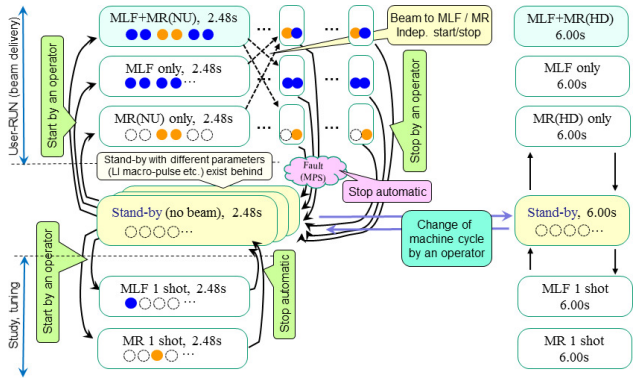

Figure 7: Transitions between beam-slot sequences.

Daily Modulation between Buildings

The length of the fiber-optic cables between buildings is about 1 km (Figure 1). One-way signal transfer takes 3-4 us. Daily time modulation, roughly 1ns, was observed between the CCB and the MR-D3 buildings. This modulation is caused by environmental temperature changes. The amount of this modulation is considered small enough and permissible for our accelerators.

Synchronization Timing

There are some exceptional trigger signals which are called "synchronization timing" [5]. For example, the extraction kicker of the RCS must be synchronized with the circulating beams, however, the standard trigger resolution (~10ns) is insufficient. The trigger for the kicker is generated by the RCS RF system. Addition to it, the MR injection kicker is triggered by the same signal with an appropriate delay. This delay is generated by a dedicated VME board, with the resolution of 2ns.

FUTURE PLANS

Evaluation of the Present System and Future

Since 2006, more than 200 VME modules have worked very well without faults, except few pieces. However, we have some problems:

- During distributing base-signals by metal cables, they suffer external noise influence from pulsed power-supplies. In an extreme case, a few meter cable suffered, especially the type-code in LVDS signal format. Ferrite cores is effective to reduce common-mode noises, but more essential solution is preferable.
- Optic devices used in E/O and O/E NIM modules, Finisar v23826 made in 2006-2010, are already discontinued. Re-producing the same modules is impossible.
- No good proposal for a small extension. When only one delay is necessary for a new component, set of a VME system and NIM modules are necessary. It requires too much space and cost.

ISBN 978-3-95450-148-9

In order to overcome above problems, we start discussion on the future possible directions. Two ideas are shown in Figure 8.

The first idea is to introduce a FPGA board with a SFP. SFP seems a safe optic device for future long availability. In addition, merging/dividing three base-signals into/from single fiber-optic cable will be possible, using a FPGA technology.

Recently, the MRF timing products have been used in many accelerators [8]. Thus, the second idea is to develop a protocol converter from the J-PARC timing to the MRF. The MRF provides small-factor platform, such as cPCI or uTCA form-factor, which would solve our space problem. In addition, direct optic-link to a front-end module (EVR) would result in an effective measure against external noises.

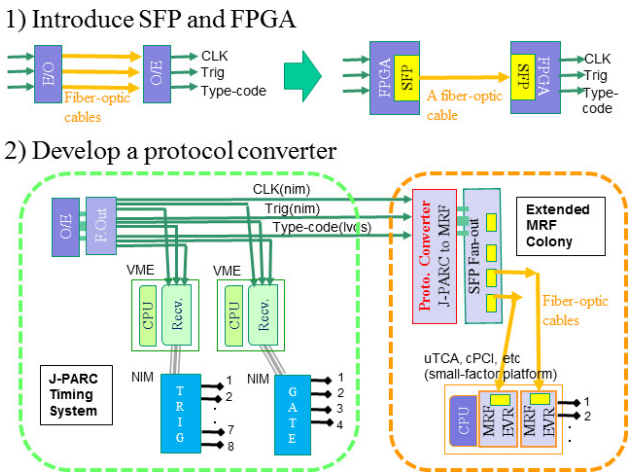

Figure 8: Two ideas for the future.

50Hz Operation of the Linac for the ADS

The ADS (Accelerator-Driven Transmutation) is an experimental facility in J-PARC. It is not constructed yet. Recently, a construction plan was approved. Additional 25 Hz beams will be needed for the ADS around 2018-2019.

In fact, the 50 Hz operation of the Linac is in the original design. The timing modules were also designed to work at the 50-Hz rate. Thus, beam-slots for the ADS can be assigned as in Figure 9.

Transitions between beam-slot sequences will be more complicated with the ADS. A plan to develop an enhanced send module with 1024 type-sequences (currently 64) is discussed.

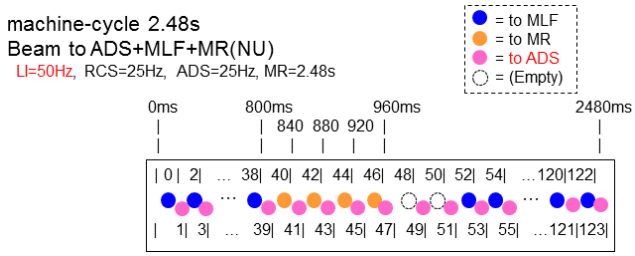

Figure 9: Plan of a beam-slot sequence with the ADS.

CONCLUSION

J-PARC Timing System hardware was developed roughly 10 years before, in collaboration with domestic companies. Software was developed by ourselves. Since 2006, the system has been used successfully in daily accelerator operations, with good enough reliability.

Recently, we have started discussions on possible migration and extension of the system for the next decade.

ACKNOWLEDGMENT

The initial development related to the send module was carried out by Y. Itoh, H. Yoshikawa, H. Sakaki and H. Takahashi. The scheme of the MR timing was designed and implemented by T. Matsumoto. We appreciate them, since these contributions were indispensable in the early development era of the J-PARC timing system. Thanks are also to Y. Sawabe, M. Kawase, K. Futatsukawa and the accelerator operators, for their continuous efforts to maintain and update the timing system.

REFERENCES

[1] J-PARC website: http://j-parc.jp/index-e.html
[2] ,S. Nagamiya, “Introduction to J-PARC”, Prog. Theor. Exp. Phys. (2012)02B001.
[3] T. Koseki and K. Hasegawa, “Present Status of J-PARC - After the Shutdown due to the Radioactive Material Leak Accident -”, IPAC’14, Dresden, Germany, THPME061, pp.3374-3375; www.JACoW.org
[4] J. Chiba et al., “Present Status of the J-PARC Control System”, ICALEPCS 2003, Gyeongju, Korea, p.1-5
[5] F. Tamura et al., “J-PARC Timing System”, ICALEPCS 2003, Gyeongju, Korea, p.247-249
[6] N. Kamikubota, et al., “J-PARC Control toward Future Reliable Operation”, ICALEPCS 2011, Grenoble, France, Oct. 2011, MOPMS026, pp. 378-381; www.JACoW.org
[7] J. Takano et al., “Residual Field Correction of Pulse Bending Magnet", JPS Conference Proceedings Vol. 8, 012023, Tsukuba, Japan (2015).
[8] MRF Website: http://www.mrf.fi

ISBN 978-3-95450-148-9