# Em# PLATFORM: TOWARDS A HARDWARE INTERFACE STANDARDIZATION SCHEME

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*Abstract*

Low current measurements developments have been pointed out as strategic for ALBA synchrotron. From the first day of operation of the seven Beamlines currently in operation ALBA Em electrometer has been successfully used. Today, the two new beamlines of Phase 2 that are being constructed and the new end stations have required specification changes in terms of increased accuracy, capability of synchronization, timestamping, management of large buffers and high performance closed-loop implementation. The scheme of full custom hardware design has been abandoned. ALBA Em# project approach has been based in the selection of industry standard interfaces: FMC boards design for custom needs, FMC carrier over PCIe using SPEC board from CERN under OHWR license, and Single Board Computer using PCIe to implement interfaces with the control system. This Paper describes the new design of the Electrometers at Alba, suited for the newer requirements, more flexible, performing and maintainable, which profits from the know-how acquired with previous versions and suits the new data acquisition paradigm emerged with the standardization of quick continuous scans and data acquisition.

## INTRODUCTION

ALBA is a 3GeV third generation synchrotron light source located in Cerdanyola del Vallès (Barcelona). ALBA houses 7 commissioned beamlines and 2 more are being constructed in the facility construction Phase 2.

Low current measurements at ALBA for diagnostic or experiment applications have been performed thanks to the successful development of a 4-channel electrometer (ALBA Em) [1]. The project started in 2011 and more than 40 units are currently working at ALBA facility since then. Due to the increase of needs mainly in the experimental area an equipment redesign need raised in 2013 (Em#) [2]. Since then the project philosophy has evolved from the full custom hardware design to be based, as much as possible, in commercial components using expected long-life interfaces. The inclusion in the equipment of a Single Board Computer (SBC) integrating part of the control system increases the complexity of the project and positively forces the incorporation of software developers in the project development stage.

With the common objective of fostering the development of Em# project a collaboration agreement has been signed between ALBA and MAX IV. The agreement could be open to other institutes or facilities interested in the project.

## HARDWARE APPROACH: DON'T SELECT THE COMPONENTS, SELECT THE INTERFACES

One of the lessons learned from first ALBA Em is that the obsolescence of commercial modules (like microprocessor cores) is a crucial factor in the equipment design. If an electronic module gets obsolete and its interface is not standard, the module replacement implies a dramatic effort of hardware redesign.

The project new approach is based first on selecting the industry standard interfaces intended to be used between the modules included in the equipment, and second selecting the modules that could fulfil these requirements. In this way, if a module gets obsolete, it can be replaced by another one using the same interfaces, and the redesign effort is lower.

In the Em# project three standard interfaces have been selected:

1. Ethernet: External communication interface from the embedded SBC to the Control System.
2. Peripheral Component Interconnect Express (PCIe): Internal interface between the SBC and the FPGA module.
3. FPGA Mezzanine Card (FMC): Interface between FPGA module and custom electronics based on VITA 57 standard [3].

The block diagram of the new hardware approach (see Fig. 1) is composed mainly by 3 well-bounded blocks, where the connections between them are the cited selected interfaces. The first block is a selected commercial fanless SBC including Ethernet and PCIe interfaces with a small 100mm x 100mm long life form factor: Intel NUC (DE3815TYBE). The second block is a FPGA module including PCIe and FMC (as carrier) interfaces: SPEC, a FPGA board developed by CERN and available under Open Hardware License (OHL) [4]. The third block contains custom electronics developed for the project. Custom electronics block includes an FMC board developed at ALBA under OHL license [5]. Its core is an isolated 4-channel 400kS/s 18 bits ADC capable of operating under ground voltage bias condition. This ADC FMC board has also a custom digital interface to control the rest of electronics; for the equipment I/O and the 4 ALBA Current Amplifiers. The 4 ALBA Current Amplifiers and the ADC of the FMC are designed to work with biased voltage ground, so the isolation is a key point with many implications in the hardware design.



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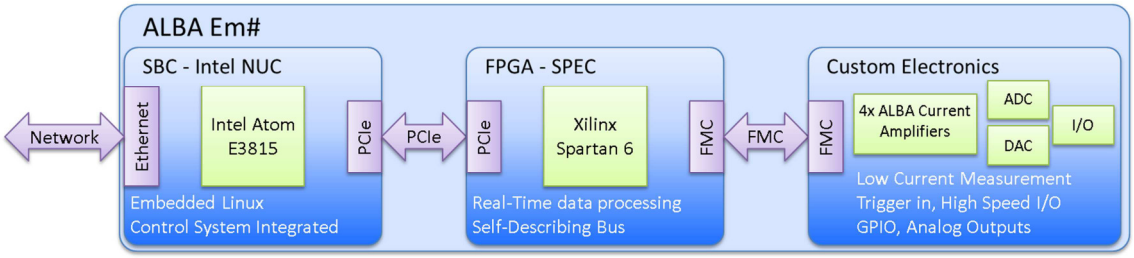


Figure 1: Em# block diagram, with the three main interfaces and elements.

## MAIN FEATURES, IMPROVEMENTS AND INNOVATIONS

### *Current Amplifier*

ALBA Current Amplifier, which is the sensing element and the equipment's core with 8 measurement ranges from 100pA to 1mA, is the only element used in this new design inherited from first ALBA Em. Its good performance, comparable with other well-known commercial current amplifiers (see Fig. 2), and its deep characterization knowledge, represents a big value in this new electrometer. An improvement to ALBA Current Amplifier is included from last version: a better thermal management in order to reduce heating and noise near the transimpedance amplifier by removing internal voltage regulator. A temperature sensor is also used for calibration and will be used for gain drifts due to heating during operation.

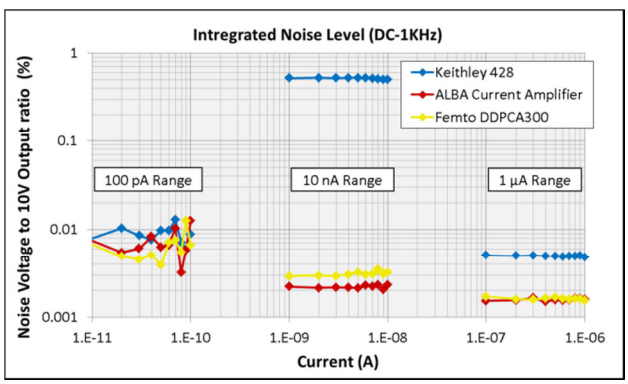


Figure 2: Integrated Noise Level comparison for 100pA, 10nA and 1µA ranges

### *Current Measurement with Voltage Bias*

In some applications in accelerators the use of isolated ground is mandatory. Among them a few even needs a high voltage ground bias to be applied. This feature that is not widely considered in most of the electrometers has been considered in Em#. In it there is the possibility of biasing the whole detector ground with an external voltage source respect to installation ground. The part of the equipment sharing the detector ground is the part in charge of the low current measurement (ALBA Current Amplifiers and ADC), which is isolated in the custom electronics area (see Fig. 4). The input low current conversion from analog to digital is done by the ADC in the isolated area, so the digital data is sent to the FPGA through digital isolators capable of 1kV withstanding. The same strategy is followed in current amplifiers control signals. The bias between two grounds is measured in the FMC by an additional ADC, and this feedback is used by the FPGA to detect overvoltage conditions and disconnect voltage bias input, for safety reasons.

### *Integrated Control System*

In first ALBA Em, the data acquisition control, data processing engine, high level functions and communication protocol with external control system via Ethernet were integrated in the same microcontroller. This strategy presented some difficulties and known functionality limitations very difficult to be overcome.

In new Em# the control strategy is clearly split: high-level functions and communication protocol integrated in SBC and low-level control integrated in the FPGA, both communicating via PCIe. The decision of centralizing high-level functionality in a SBC reduces the FPGA load with a relatively low cost.

The presence of SBC E3815 Intel Atom processor, which is much more powerful than last microcontroller, allows the control system to be designed based on layers. The design of control layers taking into account the whole hardware architecture from the beginning allows more flexibility when new requirements will rise in the future.

A custom Linux embedded distribution placed in the 4GB SBC Embedded Multimedia Card (eMMC) with a 5s boot time is nowadays used for the Em# working prototype (see Fig. 3). The Drivers low layer includes only needed drivers which give access to the hardware and its basic control. The Middleware layer contains functions, algorithms and the Em# control logic. In the Applications layer simple control applications for external user are included: display control and remote control through telnet or SCPI, which is the standard that specifies a common syntax, command structure, and data formats, to be used with measurement devices.

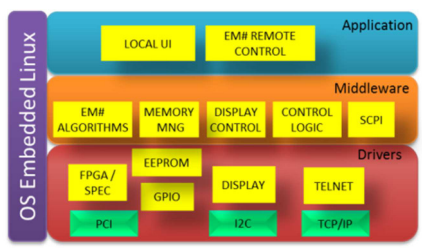


Figure 3: Control layers in SBC embedded OS Linux.



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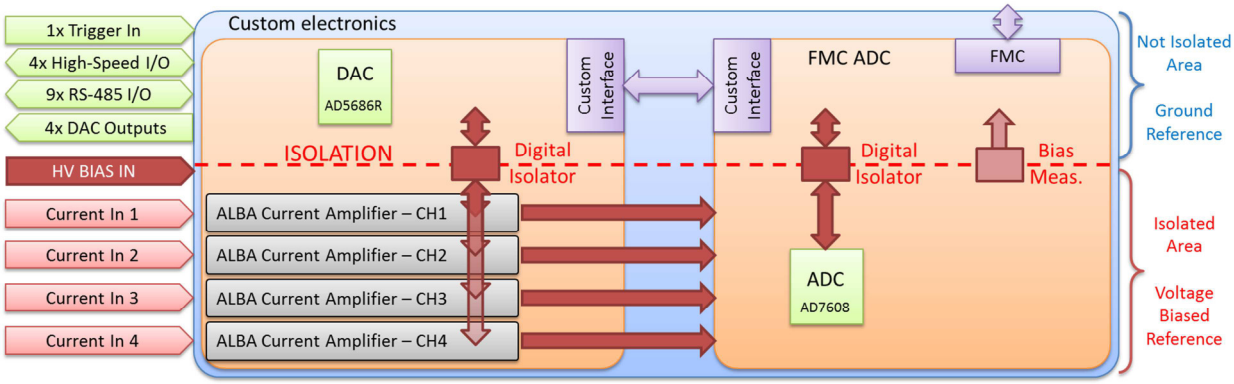


Figure 4: Custom electronics block diagram.

### *Large Acquisition Memory*

A weak point in first ALBA Em was the limited data storage capacity. A maximum vector of 1kS per channel was not enough for experiments where continuous data acquisition was required, like quick continuous scans in spectroscopy beamlines.

This situation has been dramatically improved in Em#: the SPEC board includes a 2Gb DDR3 memory directly managed by the FPGA, allowing real-time data storage without latency problems. Data will be stored in DDR3 memory in 64 bits words format, including identifier or timestamp fields. So, up to 32MS could be stored in the memory. In an application where the 4 channels from the ADC would be stored simultaneously, up to 8MS could be stored per channel.

Intel NUC SBC offers also great storage capacity due to its 8GB DDR3 RAM memory, where the data could be transferred and stored after the end of the experiment. This data transfer from SPEC DDR3 RAM to Intel NUC DDR3 RAM is done via PCIe bus after the experiment acquisition in order to avoid latency problems, as PCIe is a shared bus for all the communications between the microprocessor and the FPGA.

### *Flexible Data Processing Via Dual Bus Implementation*

The Spartan 6 FPGA contained in SPEC board is the core of the Em# low-level control, including key actions like data acquisition control, fast data storage control and data processing.

The FPGA firmware is based on the implementation of the Self-Describing Bus (SDB) specification, developed by CERN and GSI under General Public License (GPL) [6]. This specification enumerates and defines the Logic Cores synthetized in the FPGA (which are connected to a common 125MHz Wishbone bus), as well as defines their accessible registers from PCIe.

A dual bus strategy will be used in Em# (see Fig. 5). The SDB Wishbone bus, which is managed by the SBC and its latency is not predictable, will be used for the control and configuration of the Logic Cores synthetized in the FPGA. A secondary data bus internal to the FPGA will be used for the cores interconnection for high speed data transfer with minimum and reproducible latencies. This data bus is a 64 bits wide bus (data length), where the 32 data bits will be transmitted together with an 8 bits identifier and a 24 bits timestamp. Transmitter cores to the data bus will be configured via the Wishbone bus to have an identifier for all kind of data transmitted. Receiver cores will be configured to which identifiers should sniffer its data from the bus. Any processing core will be configured with the operation to perform. This general configuration scheme leads to a flexible processing strategy. For example: in the case of storing in the DDR3 a 64 averaged data from ADC channel 1, the ADC core would be configured to send channel 1 data with identifier 10. The math core would be configured to sniffer data with identifier 10, and average this data every 64 samples. The math core would be configured to send the average result with identifier 20. DDR3 managing core would be configured to sniffer data with identifier 20 to perform a write operation in the memory as a circular buffer.

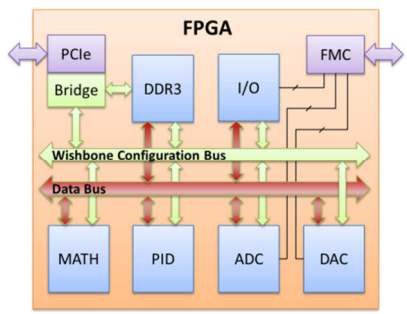


Figure 5: Block Diagram of FPGA firmware, with Wishbone Bus, Data Bus, and PCIe bridge.

### *Advanced Features*

Based on the dual bus strategy, an important application that can be implemented is the feedback as a function of the current measured by the ALBA Current Amplifiers and the ADC. The presence of four high-speed digital outputs of up to 100MHz allows for example the implementation of Voltage-to-Frequency (V2F) application, where the signal used could be directly the ADC signal or processed by the Math Core.

The four high-speed digital signals can be configured also as inputs, for example to be used as delay-

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configurable trigger inputs. An additional 200MHz bandwidth high-speed is always available as input trigger.

Nevertheless, the most expected application is the closed-loop implementation, via the usage of the four available analog outputs and a PID core. The PID input data could be directly the ADC signal or processed by the Math Core. The four analog outputs have a ±10V range generated with a low-glitch 16 bits with 100kHz bandwidth.

Em# also includes nine I/O configurable RS-485 signals that can work in unipolar or bipolar configuration, for connectivity with other equipment. The instrument is capable also to provide four +5V and 500mA outputs for external equipment supply.

## STATUS OF THE PROJECT

During last two years the Em# project has evolved from a conceptual stage to the current situation with a new hardware approach as commented previously. Nowadays the project status is in its final stage of hardware design. Thanks to the successful implementation of low-level control Logic Cores (Current Amplifiers, ADC) with SDB and its control via PCIe a working prototype has been built (see Fig. 6).

New Em# is planned to be used in the new Phase 2 beamlines and Ids currently being installed at ALBA. Different experiments are pending of its final integration in the end station to enhance its experimental results (BL22-CLAESS, BL29-Boreas). On the other hand different beam stabilization via XBPMs and monochromator piezo actuators wants to be optimized with its use.

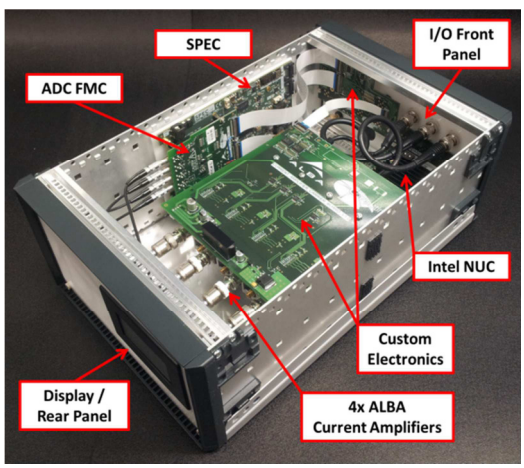


Figure 6: Em# working prototype.

### *Next Steps*

The first target to achieve is to have the complete system hardware design closed. The first Em# working series are planned to be produced in January 2016, where the functionality of first ALBA Em will be achieved with a much higher resolution. After that the project will focus on the development of the FPGA firmware for advanced features and the control system embedded in the SBC.

## CONCLUSION

After the successful conclusion of first ALBA Em project, the change from full custom hardware design to a scheme based in commercial modules using selected standard interfaces has become a successful strategy in Em#. Having the advantage of lower redesign impact due to commercial modules obsolescence, the fact of splitting the design in parts clearly separated by the selected interfaces allows a more efficient parallel tasking and an easier involvement of different development groups (hardware, FPGA firmware and software).

During last year the project has advanced with the selection of commercial modules and the design and production of custom electronics ones. The use of SDB in SPEC FPGA board and Intel NUC has started with successful results. First Logic Cores for the low-level control of the hardware have been included in the FPGA firmware as well as their control from the Intel NUC using high-level Python software. Nowadays there is a working prototype with the basic functionality of low current measurement with much improved accuracy than previous project ALBA Em. First equipment series will be produced in January 2016. After this target, where the hardware design will be closed, big effort on firmware and software development will be done to introduce important new features like big storage capability, closed-loop functionality or flexible data processing.

On the other side the collaboration agreement signed between ALBA and MAX IV for Em# project development will foster the project progress from now on due to the addition of other development groups. The inclusion of other institutes to the collaboration is open and welcome.

## ACKNOWLEDGEMENT

Thanks to all the people who worked in first ALBA Em and the knowledge learned from them, the background for Em# development is well-established. Thanks to all of them and to all the people collaborating in the current project who are not authors of the present paper.

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