NSLS-II ACTIVE INTERLOCK SYSTEM FOR FAST MACHINE PROTECTION*

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Abstract

At National Synchrotron Light Source-II (NSLS-II), a field-programmable gate array (FPGA) based global active interlock system (AIS) has been commissioned and used for beam operations. The main propose of AIS is to protect insertion devices (ID) and vacuum chambers from the thermal damage of high density synchrotron radiation power. This report describes the status of AIS hardware, software architectures and operation experience.

INTRODUCTION

NSLS-II synchrotron radiation source produces very wide spectrum ranges from IR very hard x-ray. Insertion devices (IDs) and front end devices commissioning started in November 2014 and user operation started in February 2015. The 6 NSLS-II project beamlines consist of EPU, IVU, VUV IDs. The AIS is a key machine protection system that protects vacuum chambers and front end devices from synchrotron radiation power. NSLS-II storage ring (SR) has 792 m circumference and consists of 30 double-bend achromat cells. 180 SR RF beam position monitors (BPMs) are installed around the ring, and 23 ID BPMs are installed in the straight sections. They are all fully functional. The AIS was installed in January 2014 and was successfully commissioned. It has been used in daily operation since November 2014. Recent commissioning status and results of AIS were well described in [1]. NSLS-II AIS has a state-of-the-art architecture that include 30 cell controllers (CCs) and one AIS controller based on a Xilinx Virtex-6 FPGA. The requirement for AIS is to dump the stored beam using RF interrupt within 1ms. It prevents increase of chamber temperature when orbit is mis-steered. We achieved 22 µs global BPM data transfer latency around the ring through 1 to 31 CC nodes. Each of cell controllers contains 5 Gbps transceivers running home-made serial device interface (SDI) protocol. All calculation logic is implemented using FPGA. During beam commissioning, functional test was fully completed with stored beam (1 mA ~ 300 mA) with ID gap open/close, and with ID and bending magnet (BM) photon shutters open/close. The SDI link 10 kHz packet communication and angle offset calculation results were very stable and fast enough for commissioning and user operation. In addition, the measured actual beam dump time is about 1 ms and system hardware latency time is about 200 µs.

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SYSTEM OVERVIEW

Our novel architecture of AIS is shown in Figure 1. AIS employed a 1 AIS controller, 30 CCs, 203 BPMs, 1 DCCT, 8 front end PLCs. In each cell, local SDI link connected 6 RF BPMs and additional 3 ID BPMs. AIS controller is installed in cell 23 rack group D. Each cell has its own PLC for the integration of equipment protection system (EPS) logic, for ID control and photon shutter controls. This PLC provides ID gap status, BM photon shutter status and ID photon shutter status to the local CC. Each CC communicates with its neighbor cell via 40-m multi-mode fibre optics cables. A ring topology is established by the 30 CCs with SDI protocol. The BPM position data, PLC data, and DCCT status data are delivered to the AIS controller at 10 kHz rate.

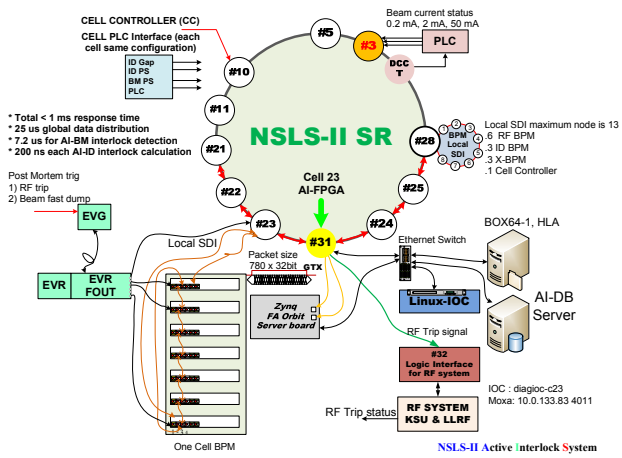

Figure 1: AI system installed layout. (Cell23: AIS and IOC installed, Cell3: DCCT controller installed, Project beamline (Cell 3, 5, 10, 11, 23, 28, 8, 18), and ABIX beamline (16, 17) IDs installed)

The AIS specification is developed following the NSLS-II synchrotron radiation protection requirements [2]:

1. Support multiple IDs and BMs.
2. The AIS controller must cover up to 64 IDs.
3. 10 kHz system monitoring and calculations.
4. Easily extensible for additional IDs which will be installed in the future beamlines.
5. Total system response time is less than 200 µs (BPM to RF trip).
6. Redundant communication.
7. Maximum fast beam dump latency time is less than 1 ms.
8. Slow beam dump time is less than 10 ms (LLRF power ramp down).

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9. Calculate angle and offset simultaneously.
10. Web-based parameters configuration and password protection.
11. Configurable operator enable/disable.
12. Diagnostic functions, such as post-mortem, can be added.
13. Time synchronization for the entire system.

Figure 2 shows the in-house designed AIS controller board and the hosting 1 U chassis (430 cm x 36 cm). AIS controller uses exactly the same hardware as the CC. The only difference is the FPGA firmware. We used same digital front end board for BPM, CC and AIS controller. However, the analogue front end circuit boards are different between these units.

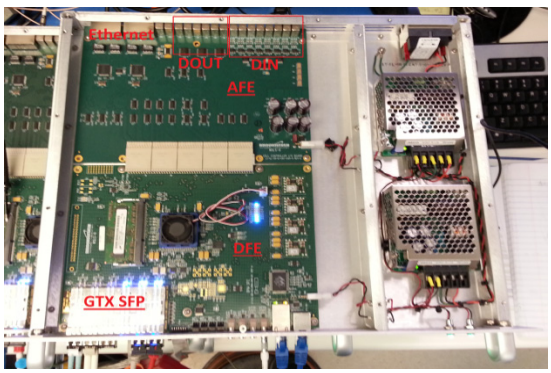

Figure 2: AIS controller

The main technical details of the AIS controller are: FPGA Virtex-6 (xc6vlx240tff1156-1), 2-Gbye DDR-3(MT8JF245664HZ-1GM1) , 5-Gbps GTX, 1-Gbps Ethernet, 16 channel 50-ohm TTL inputs, 12 channel 50-ohm TTL outputs, 16-bit 4 channel DAC.

Post-mortem (PM) Function

For a particle accelerator, PM function is widely used to diagnose the source of a beam dump, which can be caused by RF, power supplies, and other systems. The AIS controller plays the most important role for the NSLS-II PM function.

First of all, the PM trigger is generated by the AIS controller. When the AIS controller detects an abnormal beam orbit (will be discussed in details in the FGPA implementation section), or detects any system status faults (BPMs, PLCs, DCCT etc), it decides to dump the beam via RF system. In the meantime, the AIS controller sends a trigger signal to one of the distribution bus inputs of the event generator (EVG). A global PM timing event is then distributed through timing system to all BPMs, CCs, power supplies, RF systems and other systems to record the PM waveforms. We measured that the latency from the PM trigger to the BPM embedded event receiver is 5.9 µs. The latency includes AIS → EVG → global fiber fanout → 400 m fibre cable → local fiber fanout → BPM embedded event receiver.

Secondly, the AIS controller itself records the 10 kHz data for all BPMs in DDR memory as waveforms for 2 second before the beam dump and for 1 second after the beam dump. These waveforms show how the orbit changed during beam dump, and provide information to investigate which system caused beam dump.

Beam Position Monitor (BPM)

In-house designed high performance sub-nm resolution (200nm for 10Hz data) BPMs were installed and commissioned before March 2014 [3]. During the commissioning, we updated firmware several times for bug fixing and additional functions such as PM and fault detection functions. BPM provides PM waveforms for beam dump diagnostics. These waveforms include ADC raw sum (117 MHz, 256 k points), turn-by-turn x, y, sum (378 kHz, 32 k points), FA x,y (10 kHz, 10 k points).

For the AIS, the most important data from a BPM is the FA data. Each BPM has an embedded event receiver and this enables all the BPMs' FA data be synchronized within 8 ns. Each BPM has dedicated fibre optics to deliver the 10 kHz FA position data to the local CC. The total communication latency for the local 13 BPMs is 2.5 µs.

Cell Controller (CC)

The CC was originally designed for the fast orbit feedback system. Each CC has 16 50-ohm digital inputs and 12 50-ohm digital outputs. The input ports collect the following AIS-related signals and they are sent to the AIS controller via the SDI link:

- ID gap status (Open/Close)
- ID photon shutter (Open/Close)
- BM photon shutter (Open/Close)
- Canting magnet status (Normal/Fail)
  DCCT beam current level & status (0.2 mA, 2 mA, 50 mA, system fail, heartbeat)

DCCT

Beam current is measured by a DCCT which has a 50Hz low pass filter. The analogue output of this DCCT is sent to a PLC. The PLC compares this analogue signal with three pre-defined current levels of 0.2mA, 2mA and 50mA. The results are then sent to 3 digital inputs of CC at cell 3. The DCCT fault status and heartbeat signal are also sent to the digital inputs of the same CC. These digital inputs signals are delivered to the AIS controller via the SDI link.

Front End PLC

Front end PLCs collect various front end device signals, such as ID gap status, BM photon shutter status and ID photon shutter status. These signals are sent to the digital inputs of CC. In addition, the PLC calculates the overall status for the local front end using equipment-protection logic. The result bit is also sent to the digital input of CC. All the digital input signals of CCs are delivered to the AIS controller via SDI link.

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RF

The RF system receives two separate trip signals from the AIS controller. The first one is a fast dump for transmitter trip which controls the Klystron input amplifier PIN diode. The fast dump delay is about 10 µs. The second trip signal is a slow dump for low level RF ramp down in about 10 ms.

FPGA IMPLEMENTATION

For AIS controller FPGA design, Xilinx PlanAhead software package is used for project integration. Verilog HDL is used as the design language. System generator is used for angle/offset calculations. Figure 3 shows FPGA block diagram with auxiliary devices.

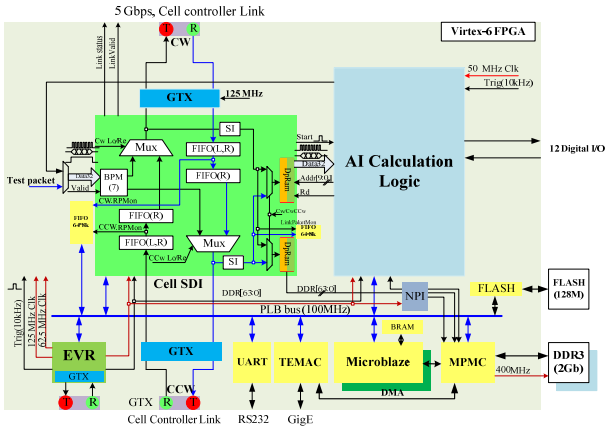

Figure 3: FPGA internal block diagram

The AIS controller obtains the data of equipment protection, front ends system, DCCT, cell controller status and BPM position at every 10 kHz from the SDI link. The RF system faults and power supply faults make a real beam orbit distortions. The overall faults are:

- BPM fault : PLL unlock, ADC saturation
- RF fault : low level RF, transmitter
- Power supply driving abnormal current: dipole, quads, sextuple, skew, correctors
- EPS/PPS malfunction detection
- BM BPMs positions out of envelop
- ID BPMs positions and angles out of envelop
- DCCT fault

AI-BM Level Comparator

AI-BM interlock logic is engaged when the beam current is larger than 50 mA. The AIS controller compares the reference orbit and the 10 kHz x/y position data of the 180 RF BPMs (6 BPMs per cell). If the difference between them exceeds acceptance envelope (+/- 5 mm in horizontal plane and +/- 3 mm in vertical plane) at any BPMs, the AIS controller generates interlock signal to trip the LLRF system and dump the beam. At the same time, the AIS controller sends the PM trigger to timing system and latches all the status data and all the calculation results.

AI-ID Angle and Offset Calculation

In order to protect the sensitive IDs and x-ray front end devices, AI-ID uses a more complicated algorithm. It requires an angle and offset calculation at each ID by using two neighbor BPMs position data. The basic angle calculation concepts are described in [2]. Here is the formula to calculate the offset and angle in H plane:

Angle = ((x2-x2Offset)-(x1- x1Offset)) * S_MRAD;
Offset = ((x1- x1Offset)*(s2-s3)+(x2- x2Offset)* S_MM;

where
x1 is BPM1 x position, x2 is BPM2 x position
s1 is BPM1 button location from center
s2 is BPM2 button location from center
s3 is centre position
x1Offset is BPM 1 horizontal geometry offset
x2Offset is BPM 2 horizontal geometry offset

The above calculation is carried out in the FPGA of AIS controller. To minimize the calculation in FPGA hardware, the two parameters, S_MRAD and S_MM, are calculated using Microblaze following the equations:

S_MRAD = (1/(s2-s1))
S_MM = ((s3-s1)/(s2-s1))

If the angle or offset are out of tolerance, the AIS controller generates beam dump signal to RF system and also generates PM trigger to timing system.

SDI Protocol for GTX Fibre Communication

At NSLS-II, a novel communication protocol called SDI is designed to support fast orbit feedback (FOFB) system and AIS. It is stable, robust and proven to have good performance during the commissioning and user operations. For SDI, the data rate is 5 Gbps and 8b/10b data encode is used. Each CC collects total of 26*32bit data packages from the local BPMs. The total global SDI data size is 26*32bit*30 = 780*32bit =3120bytes.

FOFB reads the global SDI data and uses it for feedback calculation at 10 kHz rate. The AIS controller reads this SDI data for angle and offset calculations, and for system fault detection. The global SDI data is synchronized with timing system. An SDI package has a flexible user-defined simple structure including header, data and CRC. The data packet has variable length and can be defined in Microblaze initialization routine. The SDI total communication latency was measured to be about 22 µs all of the 30 cells with the total packet size of 3120 bytes.

SOFTWARE

Software part of AIS consists of IOC and Web interface, relational database and CSS display.

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EPICS IOC

At NSLS-II, we use IBM Linux servers to host EPICS IOCs. In each cell, there is one EPICS IOC for the control of local BPMs, and one for FOFB. The AIS EPICS IOC is located in cell 23 rack group-D. EPICS IOC database provides an alarm status for the following faults:

- IOC to FPGA TCP/IP communication failure (major)
- RF dump signal (major)
- AI-ID interlock (major)
- AI-BM interlock (major)
- ID BPM fail (major)

We developed special soft IOC driver called portable streaming controller (PSC) for the TCP/IP communication between the EPICS IOC and the FPGA. The PSC uses user-defined simple protocol and driver is able to quickly transfer large waveform data between EPICS IOC and FPGA. One advantage of the PSC is that it utilizes different TCP/IP ports for FPGA to IOC streaming and IOC to FPGA streaming [4].

Web Interface and DB

Since the AIS is an equipment safety-related system, all its parameters are password protected. All AIS parameters are configured by a web based client program and it requires password for login and modifications. Only authorized people can modify the configuration and download it to FPGA memory. MySQL is used as back-end relational database to save the configuration parameters. Data service is implemented using the Django framework.

PM-Waveform Archiving

Waveform archiving software is used by CA library and saved to HDF5 file. A client program continuously monitors PM status PV. If the PM is detected, the client program reads all waveform PVs and saves them on remote file system. Currently the PM client program is archiving waveforms of RF system, power supplies, BPMs, CCs, and the AIS.

CSS Display

Control system studio (CSS) is used as high level control and monitor program. OPI page provides two different pages for AIS: one expert page and one general user page. The expert page includes all control and monitor functions while the general user page only provides system monitoring.

COMMISSIONING AND OPERATION

During commissioning we leaned important things that problem is passible by human mistake and firmware timing error. For avoid of these errors from unexpected conditions we modified epics database and BPM, AI firmware. All previous-cycle data is latched as internal registers to provide details when an interlock is detected or other failure event happens. PM waveform data are stored in local DDR-3 memory and used to provide diagnostics functions for failure analysis and event analysis. Figure 4 shows measured superconducting RF cavity field and ADC raw sum (117 MHz) signals during RF trip and beam dump.

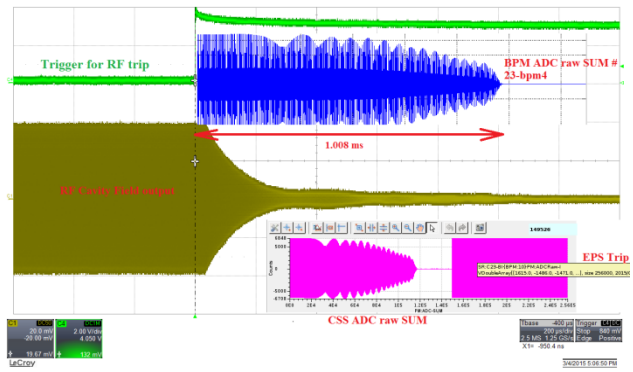

Figure 4: RF Fast dump latency measurement (acting time is 20 µs, total beam loss time is 1 ms)

SUMMARY

In 2009, we started the hardware and firmware design for BPMs, FOFB and AIS with SDI protocol. We achieved remarkable performance: 22 µs global SDI communication latency, 46 µs latency from BPM to AIS output signal for RF dump, and 5.9 µs of global PM trigger latency. We confirmed there is no error in SDI communication between 30 CC nodes and one AIS controller. In September 2014 we started AIS commissioning with up to 150 mA beam current and ID operations. In September 2015 we confirmed all designed functions with 300 mA beam current and top-off operation. All system functions and reliability are proven during the commissioning and operation in the last two years. The AIS will include more beamlines when the ABXI and NEXT beamlines are built until 2018.

ACKNOWLEDGMENT

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