TANGO INTEGRATION OF A SPECIFIC HARDWARE THROUGH HTTP-SERVER

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Abstract

MAX IV are new synchrotron third generation. MAX IV synchrotron consist of 1.5 GeV storage ring, 3.0 GeV storage ring and linac; it is located in Lund, Sweden. Structure of storage rings contains several pulse magnets (kicker and pinger). Control system of pulse power supplies based on LTR crate with several modules (ADC, DAC, input/output registers etc.). LTR crate is a product Russian firm L-CARD. In order to communicate with crate native LTR-server is used. LTR-server is a Windows application based on use of sockets. Control system of MAX IV and Solaris uses TANGO. For integration LTR-crates in final structure, special software gateway is used. This gateway is a set of several specific Windows applications implemented by using Qt5 libraries. Gateway allows communicating TANGO-server with crate through built-in HTTP-server.

SPECIFIC HARDWARE

The MAX IV facility included two storage rings for the production of synchrotron radiation: the 3 GeV and 1.5 GeV storage rings [1]. Both rings will be operated with top-up shots supplied by the 3.5 GeV MAX IV linac acting as a full-energy injector at up to 10 Hz repetition rate. At the commissioning phase, the single dipole kickers will be used for the injection in the both rings. In addition, pulsed vertical kickers (pingers) are needed for performing tests with the stored electron beam.

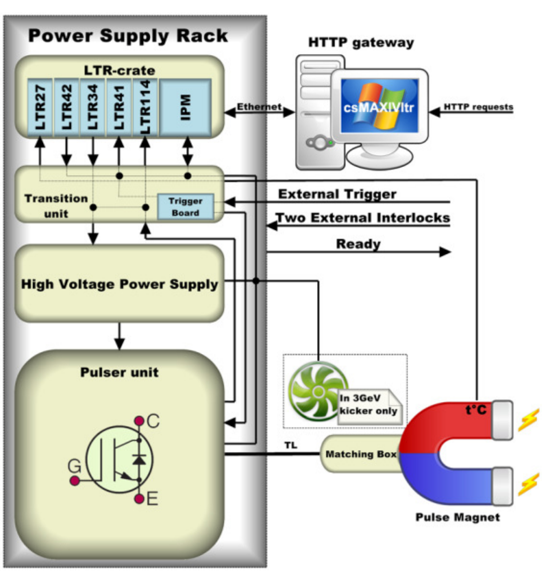

Figure 1: General pulse power supply structure.

Table 1: Pulse Magnet Systems Specifications

	1.5GeV		3GeV	
	kicker	pinger	kicker	pinger
Integrated field, Gm	143	75	450	110
Peak current, A	1060	2050	3600	2600
Pulse length, µs	0.64	0.64	3.5	3.5
Maximum rep. rate, Hz	10	1	10	1
Pulse to pulse timing,ns	±5	±5	±5	±5
Pulse to pulse repeatability, %	±0.1	±1	±0.1	±1

The requirements for the pulse magnet systems are listed in Table 1. Structure of all system (power supply with control electronics and magnet) are illustrated on Fig.1.

Control system of the pulse power supply based on 19" LTR-crate (LTR-EU-16). It is a product of a Russian firm L-CARD (http://lcard.ru). Base structure of the LTR-crate are represented on a Fig. 2.

This crate include FPGA Cyclon EP1C3 for

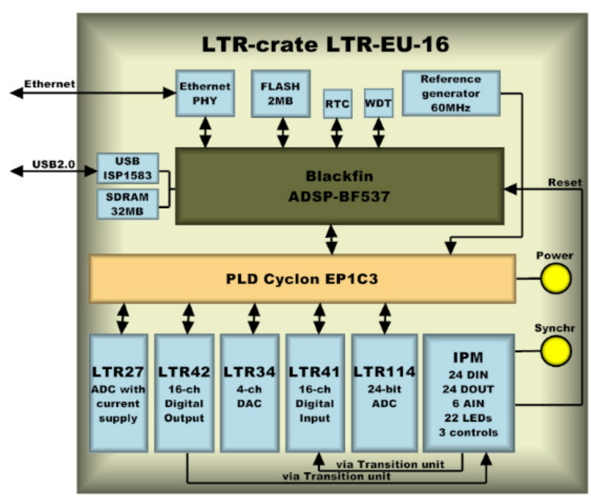

Figure 2: Power supply control system (LTR crate with modules) block diagram.

communication with installed in crate modules via proprietary interface and digital signal processor Blackfin ADSP-BF-537 for preliminary data processing. DSP operates under control of Visual DSP++ Kernel (VDK) [2]. Sources of a DSP firmware in free access and can be modified for individual requirements. Crate can communicate with PC over USB2.0 or Ethernet (TCP/IP) via L-CARD specific protocol.

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The following modules are installed in LTR crate:

1. LTR41 (16 channels digital input module);
2. LTR42 (16 channels digital output module);
3. LTR114 (24 digits ADC module);
4. LTR34-4 (4 channels DAC module);
5. LTR27 (thermo ADC);
6. IPM (Interlock Processing Module);

All modules (except IPM) was produced by L-CARD. Interlock Processing Module was made in Budker Institute of Nuclear Physics. It communicate with LTR-crate over digital inputs/outputs by LTR41/42. Brief characteristics of modules and their targets of using are listed below.

LTR41 Digital Input Module

LTR41 is 16-channels input module for TTL/CMOS-signals (with 5 V-logic) and also for current logical signals (up to 25 mA) with per-channel galvanic isolation. It is used to synchronize and to get current states and interlocks values from Interlock Processing Module.

LTR42 Digital Output Module

LTR42 is a 16-channels output module with per-channel galvanic isolation. It is used to send control commands to the interlock processing module and to generate "heartbeat" signal, which is used by the algorithm of checking the status of connection to control PC.

ADC Module LTR114

LTR114 module is a 24-digits ADC with sampling frequency up to 4 kHz, differential input and dynamic commutation to 16 channels. It has software controlled input sub-ranges ±10 V, ±2 V, ±0.4 V independently for each channel. LTR114 is used to measure high voltage and to monitor settings of the HVPS (voltage and current).

DAC Module LTR34-4.

LTR34-4 module is a 4-channel 16-digits DAC with output frequency up to 500 kHz in voltage range from -10 V to +10 V. It is used to set up the HVPS output voltage and current values.

Thermo-ADC LTR27

Unit LTR27 is a mezzanine module with possibility to install up to eight submodules. In current configuration a single submodule H27-R250 for resistances measurement is used. Frequency of data yield is up to 100 Hz. The unit is used to monitor the temperature of the magnet’s vacuum chamber by measuring resistance of thermoresistor Pt100.

CONTROL SYSTEM SOFTWARE

L-CARD produce software package for operate with crate and modules. First, this package include LTR-server (for Windows PC) and ltrd daemon (for Linux PC). These applications necessary for initializing operations, obtaining data from crate in uniform format and allocating data according to list of modules. In addition, software package include necessary library (C++/LabView) for implementation individual application for communicate with modules over LTR-server or ltrd. There is utility named UTS for test purposes and there is L-Graph2 application for collecting and visualization data from various ADC.

Set of modules is a low layer control and monitor system of pulse power supply. High layer is a Tango server with appropriate operator screen. Therefore middle layer for communicate Tango server with LTR-crate is necessary. This middle layer was realized in BINP and named csMAXIVltr. Main goal of this software part is be gateway between Tango and LTR. Moreover, csMAXIVltr provide several procedures for normal work of the power supply.

csMAXIVltr consist of four Windows application:

1. Starter, which start and control all other applications;
2. LTR-target – main application, which communicate with LTR-server;
3. HTTP-server – for communicate with Tango server;
4. LTR-server – L-CARD application for communicate with LTR-crate.

Basic structure of the csMAXIVltr are presented at Fig. 3.

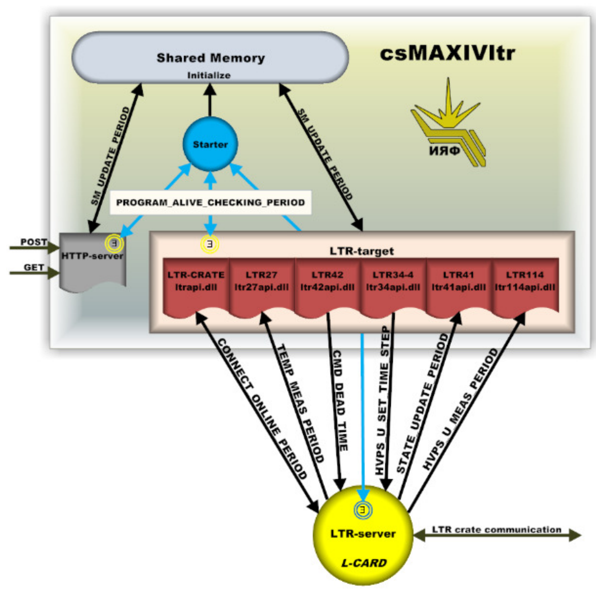

Figure 3: Basic structure of software gateway.

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All BINP parts of the csMAXIVltr was realized with Qt5 framework for operate on Windows machine. Starter, LTR-target and http-server interact together over shared memory with specific period (SM_UPDATE_PERIOD) which amount approximately 100 ms. Each module in LTR-target operate in its thread and interact together with QT native SIGNAL/SLOT mechanism.

Http-server

Http-server based on QHttpServer by Nikhil Marathe [3]. This csMAXIVltr part provide access Tango server to main actions (switch on/off, reset), settings (current/voltage), states and interlocks. Procedures for writing and reading of csMAXIVltr internal settings were added in last version.

Http-server ensure the fulfilment of two basic methods: POST and GET. POST method are used for control pulse power supply: switch on/off high voltage power supply, reset interlocks, disable or enable trigger and write voltage and current settings to HVPS. Each POST-request should contains single command. So if it is necessary to send a number of commands to the system then the sequence of POST-requests should be generated. If POST-request contains a few commands then only the first command is processed and other are ignored.

GET method are used for reading various measurements (voltage from divider, feedback levels, temperature), states and interlocks. Moreover, by GET method operator can modify internal csMAXIVltr settings (IP address, timeouts, average size and many other).

Http-server responding with identical answer on POST or GET request. This response consist of two parts: simple html-page (yellow on the Fig. 4) and last line with all required parameters (green on the Fig. 4). “Yellow” part required only for debugging or testing without Tango operator screen. “Green” part are implemented in POST data format – …&ParameterName=ParameterValue&… This part formatted like comment in html page.

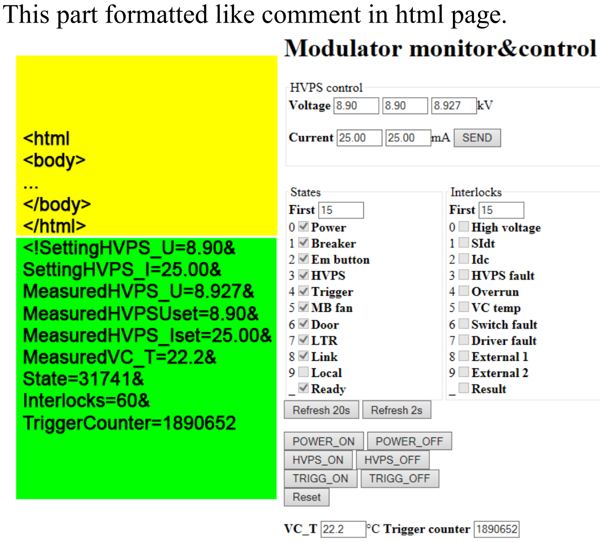

Figure 4: Typical Http-server response.

Read request structure of a csMAXIVltr parameter via GET are look like http:\\x.x.x.x\~PATH??

Write request structure of a csMAXIVltr parameter - http:\\x.x.x.x\~PATH=VALUE! where PATH is variable combined from APPLICATION_NAME and PARAMETER_NAME.

In additional http-server supports authenticate header for security operate with control system. Login and password can be changed by configuring csMAXIVltr.

Tests

Several basic tests was performed for operability checking of the system. Apache Benchmark output are represented at Listing 1.

```
This is ApacheBench, Version 2.3 <$Revision: 1663405 $>
Copyright 1996 Adam Twiss, Zeus Technology Ltd, http://www.zeustech.net/
Licensed to The Apache Software Foundation, http://www.apache.org/
Benchmarking 192.168.1.6 (be patient)
Server Software:
Server Hostname:     192.168.1.6
Server Port:         80
Document Path:       /
Document Length:     0 bytes
Concurrency Level:   10
Time taken for tests: 3.627 seconds
Complete requests:   1000
Failed requests:     0
Non-2xx responses:   1000
Total transferred:   110000 bytes
HTML transferred:    0 bytes
Requests per second: 275.73 [#/sec] (mean)
Time per request:    36.267 [ms] (mean)
Time per request:    3.627 [ms] (mean, across all concurrent requests)
Transfer rate:       29.62 [Kbytes/sec] received
Connection Times (ms)   min mean[+/-sd] median  max
Connect:        0   0  0.4    0    1
Processing:    32  36  1.8   36   44
Waiting:       32  36  1.8   35   44
Total:         33  36  1.8   36   44
Percentage of the requests served within a certain time (ms)
  50%   36
  66%   36
  75%   37
  80%   37
  90%   38
  95%   39
  98%   42
  99%   43
 100%   44 (longest request)
```

Listing 1:Apache Benchmark output.

Control test results are represented on a Fig. 5. Histogram corresponds to result of write “action” command tests. Delta is time between operator action (mouse button click on “Reset” button at html page) and actual control system operation (reset interlocks by IPM). This time summarize three large latency: shared memory update time by http-server (≤80ms), read time from shared memory by LTR-target (≤80ms) and send time to IPM over digital output module by using special robust protocol (≤160ms). These times can be decreased by configuring csMAXIVltr, but this action increase CPU load.

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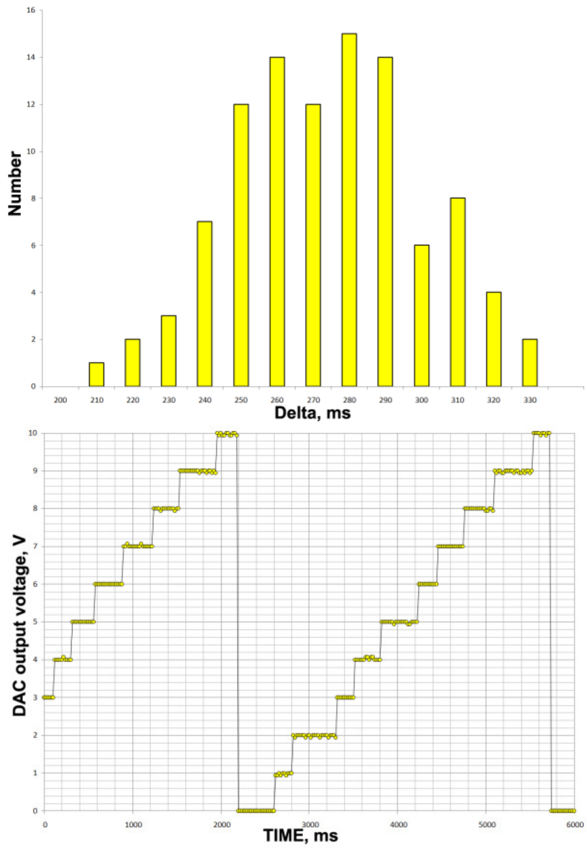

Figure 5: Write command test results.

Upstairs graph represent continuous sequence of voltage setpoints from zero to 10 Volts with 300 ms time step.

TANGO VIEW OF PULSE POWER SUPPLY

Tango-server for pulse power supply was realized by Cosylab. It contains 29 attributes for operator display level and additional 35 attributes for expert. Majority of operator view attributes (20) are Boolean which indicate state or interlock.

Power supply control state machine are illustrated at Fig. 6. This diagram not include UNKNOWN and INIT states because they define only internal Tango server implementation. All other state defining from status of the pulse power supply.

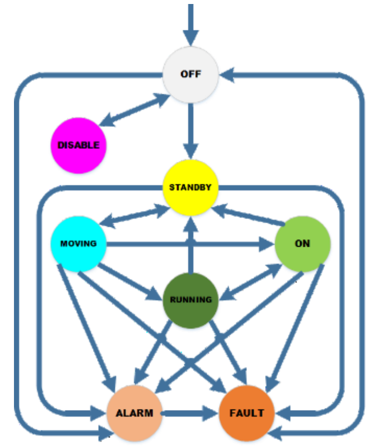

Figure 6: Power supply state machine in Tango view.

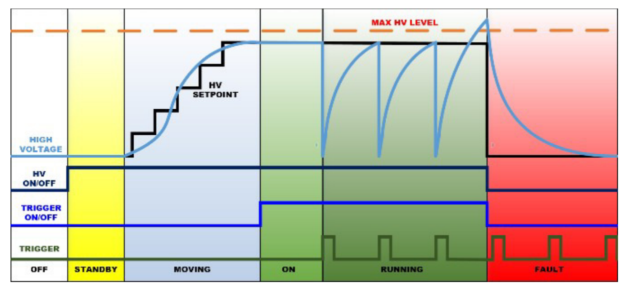

Figure 7: Basic conditions for Tango state definition.

At the Fig. 7 are represented basic conditions for Tango main states definition. Trigger pulses are external synchro signal for power supply start. FAULT state condition came when high voltage exceed legal level for example.

Software gateway based on the very simple http-server allow to link LTR-crate with Tango approach for successfully control of pulse magnet power supplies.

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