PANDA MOTION PROJECT - A COLLABORATION BETWEEN SOLEIL AND DIAMOND TO UPGRADE THEIR 'POSITION AND ACQUISITION' PROCESSING PLATFORM

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Abstract

Synchrotron SOLEIL and Diamond Light Source are two third generation light sources located respectively in France and the UK. In the past 5 years, both facilities separately developed their own platform permitting encoder processing to synchronize motion systems and acquisition during experiments, SPIETBOX by SOLEIL and ZEBRA by Diamond. New operational requirements for simultaneous and multi-technique scanning, and support of multiple encoder standards have been identified by both institutes. In order to address these a collaborative project has been initiated between SOLEIL and Diamond to realize a new 'Position and Acquisition' processing platform, called PandA. The PandA project addresses current systems' limitations in terms of obsolescence and need for more processing power. Its design is going to be a 1U standalone system powered by a Xilinx Zynq SoC to implement a configurable set of logic functionalities. It will provide a flexible and open solution to interface different third party hardware (detectors and motion Controllers). This paper details the organization of this collaboration, sharing technical leadership between both institutes and the status of the project.

COLLABORATION MANAGEMENT

SPIETBOX [1] and ZEBRA [2] were designed in-house by SOLEIL and Diamond respectively, and both have been integral part of beamline operations, and proven useful for synchronising various equipment and for position capture. One application is to synchronize detectors with optics that select the photon energy of the beam to acquire only useful data, another one is facilitating the use of continuous scanning for faster acquisition in 2014. Both institutes share the same vision for a new motion control and data acquisition architecture. So SOLEIL and Diamond have gone into a collaboration to re-design and improve these platforms with following guidelines:

- Both institutes want to standardize hardware, in order to reduce number of systems which need to be developed and maintained by the support staff.
- Develop a ready to use and complete solution, in order to install quickly and easily all the hardware and software components.

The main goal of the collaboration was to share resources and experiences between both synchrotrons for the development. The first step was to understand existing skills and human resource availability at both institutes and agree on sharing the responsibilities of each task at design level as shown in Table 1. We decided to manage the work through regular video conference meetings every two weeks, face-to face meeting every 3 months, as well as sharing minutes and documentation over a private Github repository. Once the organization was set-up, a set of hardware, firmware and software specifications were defined as described in the following sections. It is agreed that the hardware developed during the course of the collaboration would be developed under the CERN Open Hardware (OHW) Licence [3] and released on the public OHW repository following completion of the project. Both parties would also have the option to engage third parties to commercialise the resulting project.

Table 1: Task Sharing Between Project Partners

Task leadership	DIAMOND	SOLEIL
Project management	X	
HW, FW specifications	X	X
Schematic Design		X
PCB Layout		X
Mechanics		X
FPGA – Zynq Processor Design	X	
FPGA – Zynq Logic Design	X	
Linux Kernel Development	X	
Linux Application Development	X	
TANGO interface		X
EPICS interface	X	

HARDWARE ARCHITECTURE

New applications [4], operational feedback from beamline scientists and from the Flyscan project [5] identified the following requirements to address limitations of existing SPIETBOX and ZEBRA solutions:

- Multi Channel TTL and LVDS I/Os for synchronous triggering and clocking with higher timing resolution.
- 4-Channels of encoder interface I/Os, supporting a wider range of protocols including Incremental, Absolute, EnDat and BiSS.
- 2-Channels of SFP Gigabit Transceiver interface for IpBus, Timing System, Diamond Communication Controller [6] or custom high-speed serial connectivity.

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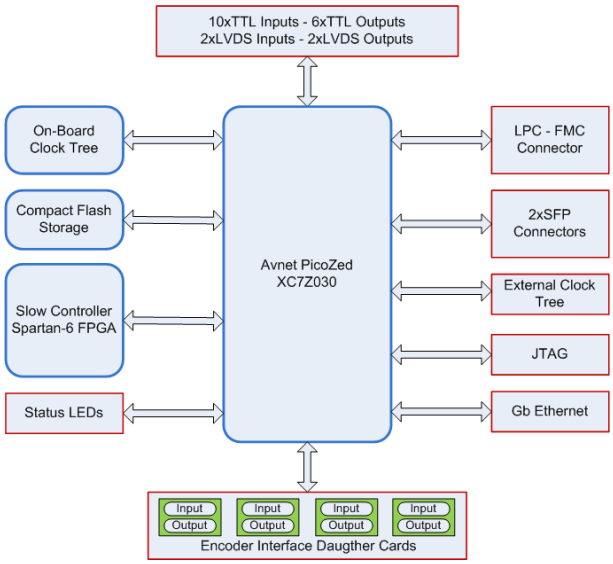

Figure 1: System Architecture.

- A fully compliant Low-Pin Count FMC slot for interfacing to analog and digital off-the-shelf boards or custom I/O modules.
- A Gigabit ethernet connectivity for control systems integration and high-speed data acquisition.
- A capable FPGA-SoC device for significant improvement of existing processing, programmable functionality and tighter system integration.

The proposed hardware architecture in Fig. 1 gives us a platform we can develop specific solutions with simple, reliable and durable tools. The platform is suitable in particular for applications where it is generally necessary to synchronize a range of equipment, which are managed by implementing the process at low level.

At the heart of the system architecture is the PicoZed [7] System-On-Module as shown in Fig 2. The PicoZed module contains Xilinx Zynq-7030 All Programmable (AP) SoC and the common functions required to support most SoC designs, including memory, configuration, ethernet, and clocks. It provides easy access to over 100 user I/O pins through three I/O connectors on the rear of the module.

A modular approach to the hardware design was taken by:

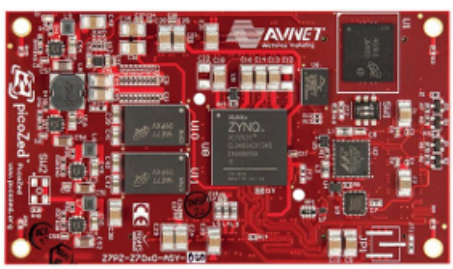

Figure 2: Avnet Picozed SOM.

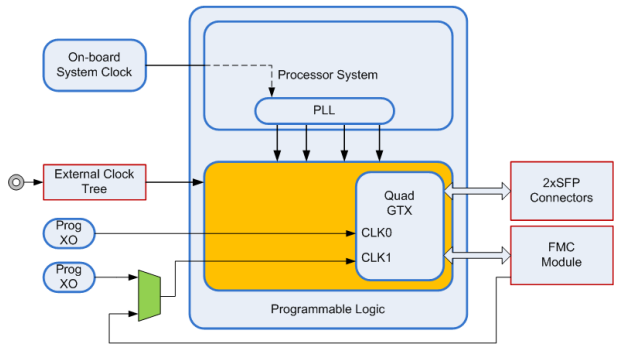

Figure 3: PandA Clocking Scheme.

- Using daughter cards for the encoder interface electronics permitting custom solutions, and to accelerate the development process. The current daughter card has been designed with pin-compatibility with the SOLEIL and Diamond motion controllers.
- Adding an industry standard fully-compliant Low Pin Count (LPC) FPGA Mezzanine Connector (FMC) to the architecture to enable analog I/O capability by using 3rd-party products [8] or custom modules.

In order to achieve the maximum flexibility that PandA can offer in terms of application support, a clocking architecture is built for clocking user programmable logic and Gigabit transceivers as shown in Fig. 3.

One of the drawbacks of modern programmable SoC devices is the limitation in terms of user I/O count. In our case, PicoZed module provides 135 user I/Os which is not enough to cover all the connectivity required by the specifications. To address this limitation, another lower-end FPGA device with multiple user I/Os is used to handle slow control functionality of various on-board devices. The communication between the main XC7Z030 Zynq device and slow control FPGA is achieved using an SPI-like custom interface.

PandA will consists of a 1U metal box, with BNC and LEMO connectors for single ended, differential signals and Gigabit Ethernet on the front panel. 15-way D-type connectors for RS485 encoder signals and power on the back panel.

FIRMWARE CAPABILITIES

PandA firmware functionality was designed to achieve full configuration flexibility and tight control system integration. The firmware implements a list of logical functions, a range of position compare functionality, high-throughput position capturing, multi-gigabit serial interconnections, and Arm processor interface.

Logic Operations and Position Based Blocks

A list of logical functions that had already been implemented by existing solutions was reviewed and following improved blocks were defined for PandA:

- Function generators to implement any 5-input boolean function.

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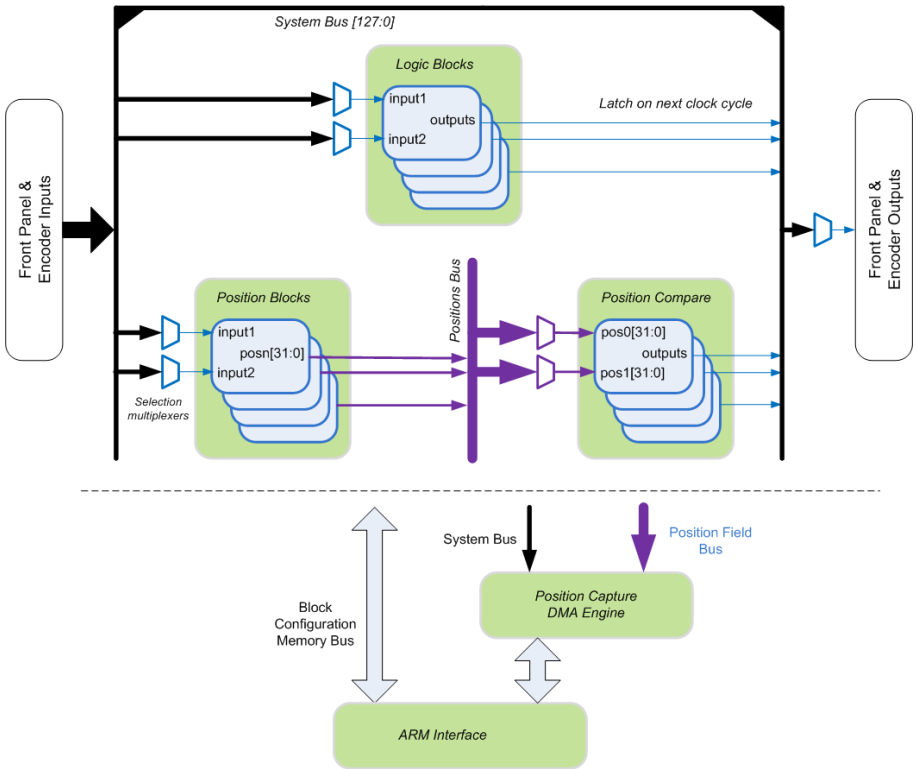

Figure 4: PandA Firmware Architecture.

- Set/Reset Gate blocks with configurable inputs, and an option to force its output independently.
- 32-bit Pulse divider with programmable divisor and two pulse outputs (divided and non-divided).
- Pulse Generator blocks to produce configurable width and delayed pulses triggered by its input and also able to handle pulse trains.
- Sequencer blocks to perform automatic execution of sequenced frames to produce timing signals.
- Programmable clock generators.

Similarly, a wide range of position based blocks are defined:

- Encoder Input/Output blocks supporting multiple encoder protocols.
- Quadrature Input/Output blocks to enable of any discrete signal on the system for quadrature operations.
- Counter/Timer blocks to implement multi-channel 32-bit up/down counters synchronous to system clock.
- Analog input/outputs upto 8-channels through FMC module connectivity.

To achieve connectivity between all design blocks, two internal buses are defined. The System Bus is a 128-bit wide register is composed of concatenating all physical I/Os, and registered discrete outputs from logic and position-based blocks. Similarly, all 32-bit outputs of the position based blocks are concatenated together to create the 1024-bit wide (32x 32-bit) Position Bus.

By connecting the input of any logic block to the system bus via a 128x1-bit multiplexer, it becomes possible to cascade multiple blocks to achieve the desired functionality. Each physical output is also taken from the system bus in the same way (see Fig. 4). Position Bus feeds all the 32-bit position inputs of all position compare blocks using 32x32-bit multiplexer so that position compare processing can be done on encoder, timer or analog input values.

Position Compare and Capture

The position compare blocks in PandA are designed to be able to generate a stream of trigger pulses, which can be position based, time based, analog input based or externally triggered. A new feature added to the position compare functionality is the ability to use LUT-based arbitrary arrays of position or time points instead of regularly spaced series of values. This facilitates:

- Position based capture – where output pulses are generated when the encoder position reaches a certain value, or series of values.
- Time based capture – where output pulses are generated at regular time intervals, storing the encoder positions as well.
- Analog input based capture – where output pulses are generated when analog input position reaches a certain value, or series of values.

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- External trigger capture – where the motion controller stores the encoder position on an external trigger signal.

By cascading multiple position capture blocks, it is possible to mix modes together, such as outputting a time based pulse stream within a series of position based gates.

A central position capture block is responsible for capturing user-defined fields across the design including timestamps, encoder values, analog input values, counters and system status on trigger events. The captured data is DMA transferred into the system memory, and read out via gigabit ethernet interface.

Multi Gigabit Connectivity

The 3-channels of Multi-Gigabit Transceivers (MGTs) on the Zynq device are brought onto the front panel through SFP connectors. Along with the flexible clocking architecture in Fig. 3, these MGTs enable implementation of following interfaces on PandA for wider-level connectivity.

- Diamond Communication Controller: Light weight, low latency and high reliability data distribution.
- IPBUS: Simple, reliable, UDP/IP based protocol for controlling hardware devices.
- Micro-Research Event Receiver: to recover timing events and clocks distributed across the event network.

Processor Interface Logic

The processor interface logic handles communication with the host on Zynq-Arm Processor System for control and data acquisition purposes. The Zynq-Arm will run linux and use a dedicated linux device to tightly integrate with the FPGA logic. This will be through

- A dedicated address space on the host system memory enable direct access to each firmware block's configuration and status registers.
- A Write DMA master engine to transfer position capture data onto the system memory in real-time. Data rates up to 128MB/sec (capturing up to 32 position fields at 1MHz pulse rate) are envisaged.
- A Read DMA master engine for synchronous reading of user-defined arrays for position compare operation. The length of user defined arrays being limited to 1MSamples.

CONTROL SOFTWARE ARCHITECTURE

Figure 5 depicts standalone software architecture for PandA project. The kernel driver provides control and status register access to system blocks, and interface with the DMA engines for synchronous read/write data transfers. It is wrapped by a TCP Server that implements custom protocols over two channels for data and control interfacing. It is our intention that PandA will be integrated either with an EPICS IOC, a webserver interface, or with a separate TANGO server.

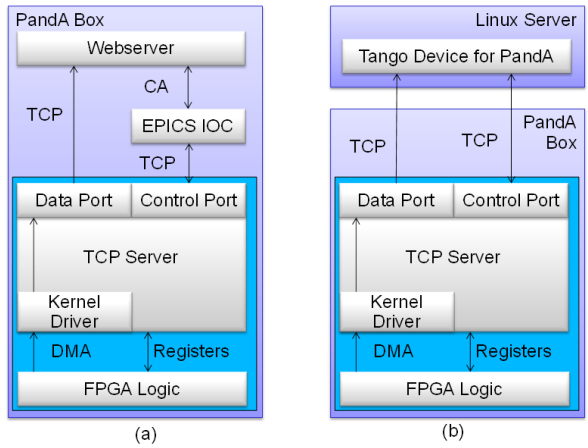

Figure 5: Software Architecture for (a) Diamond, (b) SOLEIL.

SUMMARY

Diamond and SOLEIL share the same vision of motion control architecture and have started collaboration for development of a common platform for Position and Acquisition of encoder sensors (PandA). Following agreement on the hardware, firmware and software specifications, both parties started design work mid-2015. Using commercial products, as much as possible, allows efforts to focus on applications requirements and saving time in development. The initial design and development phase is planned to be completed in the first quarter of 2016, with a provision of having prototype units during mid-2016.

REFERENCES

[1] Y.M. Abiven, et al., *SPI Boards Package, A New Set Of Electronic Boards at Synchrotron SOLEIL* , Proc. of ICALEPCS'2011, Grenoble (France).

[2] T. Cobb, Y. Chernousko and I. Uzun, *ZEBRA: A Flexible Solution for Controlling Scanning Experiments*, Proc. of ICALEPCS'2013, San Francisco (USA).

[3] CERN, *Open Hardware License*, `http://www.ohwr.org/projects/cernohl/wiki`.

[4] R.D. Walton, *Mapping Developments at Diamond*, THHB3O01, these proceedings, ICALEPCS'2015, Melbourne (Australia).

[5] N. Leclercq, at al., *Flyscan: a Fast, Simultaneous and Multi-technique Data Acquisition Platform for the SOLEIL Beamlines*, WEPGF056, these proceedings, ICALEPCS'2015, Melbourne (Australia).

[6] I. Uzun, et al., *Initial Design of the Fast Orbit Feedback System for DIAMOND Light Source*, Proc. of ICALEPCS'2005, Geneva (Switzerland).

[7] Avnet, *Picozed Product Brief*, `http://zedboard.org/product/picozed`.

[8] D-TACQ Solutions, *ACQ430FMC: 8 channel simultaneous sampling digitiser*, `http://www.d-tacq.com/modproducts.shtml`

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