DESIGN AND COMMISSIONING RESULTS OF MICROTCA STRIPLINE BPM SYSTEM*

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Abstract

The Linac Coherent Light Source (LCLS) is a free electron laser (FEL) facility operating at the SLAC National Accelerator Laboratory (SLAC). A stripline beam position monitor (BPM) system was developed at SLAC [1] to meet the performance requirements necessary to provide high-quality stable beams for LCLS. This design has been modified to achieve improved position resolution in a more compact form factor. Prototype installations of this system have been operating in the LCLS LINAC and tested at the Pohang Accelerator Laboratory (PAL). Production systems are deployed at the new PAL XFEL facility and at the SPEAR storage ring at the Stanford Synchrotron Radiation Lightsource at SLAC. This paper presents the design and commissioning results of this system.

BACKGROUND

At LCLS, stripline BPMs measure the transverse position of the electron bunch in the injector, Linac, and transport lines. Each BPM is instrumented with a SLAC-designed chassis that houses analog conditioning electronics, a digitizer, and a CPU. After digitization, the processed data is transmitted over a dedicated network to a VME processor that calculates pulse-by-pulse beam position. An online calibration scheme injects a tone into the system between beam pulses in order to compensate for gain variation and drift. This process occurs at the beam rate, which is 120 Hz.

For recent projects, it became desirable to use electronics in a smaller form factor while maintaining the performance standard of the LCLS design.

SYSTEM DESIGN

A new system was developed, using the MicroTCA (Micro Telecommunication Computing Architecture) crate architecture. In this system, electronics for several BPMs are housed within a single crate, with digitizers located in the front of the crate and the analog conditioning electronics in the rear. Digitized data is transferred along the PCIe backplane to the CPU for processing.

The first version of this system [2] was tested in the LCLS Linac and found to meet the performance requirements. Two of these BPMs have been deployed in a SPEAR transport line.

Later, this design was further modified to achieve improved position resolution for the PAL XFEL facility. Revised electronics, including a different operating frequency, larger bandwidth, and faster digitization rate, provide position resolution improved by a factor of two. Prototypes of this system were tested in the SLAC Linac and at the PAL Injector Test Facility (ITF). Hardware design details presented in this paper are for this improved design.

Analog Front End

The analog front end (AFE) is used to reduce the signal bandwidth and set the signal level before digitization. To achieve the desired system resolution at low bunch charge, it is important to minimize losses in the system. This is most important in the signal cables and the AFE components up to the first amplifier.

The SLAC-designed AFE contains two stages of amplifiers and attenuators. The attenuators can be adjusted from the control system to maintain reasonable signal level when the bunch charge changes. The bandpass filters select a processing frequency of 300 MHz with a bandwidth of 30 MHz. Figure 1 shows a block diagram of a single input channel of the AFE.

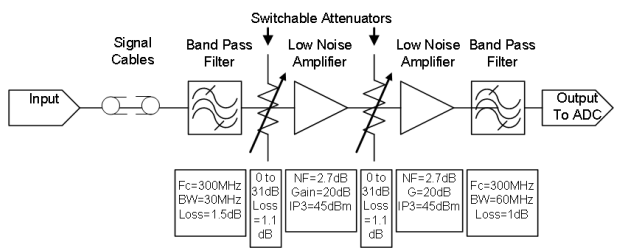

Figure 1: Analog Front End block diagram.

As in the LCLS system, the AFE performs a self-calibration process between beam pulses. A 300 MHz tone is injected into a single stripline and the coupled response is measured from the two adjacent striplines. This is performed for both the horizontal and vertical transverse planes. The calculated calibration ratios are applied to the beam position calculation to compensate for thermal drift and gain variation among channels. Figure 2 shows a block diagram of the calibration scheme.

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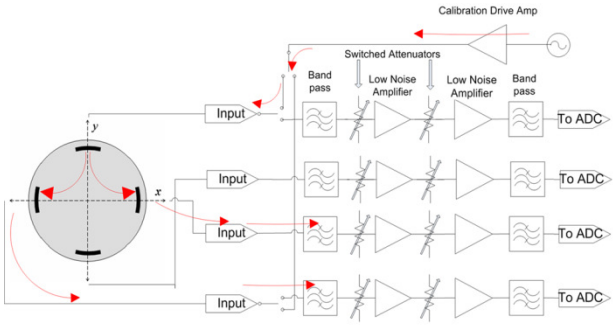

Figure 2: Calibration scheme.

Digitizer

To meet the resolution requirements, the analog-to-digital converter (ADC) must provide sufficient effective number of bits and signal-to-noise ratio. A commercial off-the-shelf product, the Struck SIS8300, was selected.

It is important to select a digitization rate that centers the signal well within the Nyquist zone. This reduces unwanted signal leaking in from neighboring zones, which decreases signal quality. This effect is also improved by good filtering and selection of analog bandwidth. In this system, the 300 MHz BPM signal is undersampled at 250 MSPS, which centers the 30 MHz-bandwidth aliased signal well in the first Nyquist zone. Figure 3 shows the 300 MHz BPM signal, the 250 MSPS digitization rate, the Nyquist zones, and the frequencies of the aliased BPM signal.

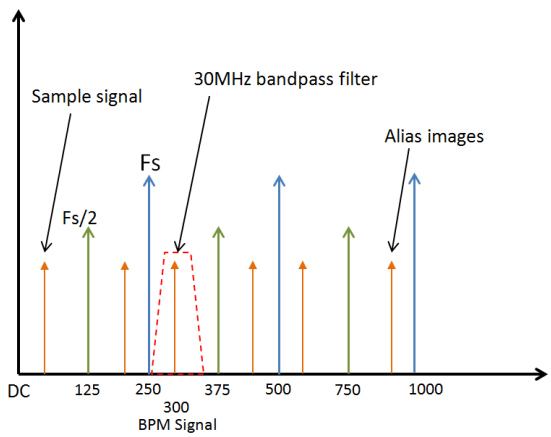

Figure 3: Nyquist zones and aliased signals.

Timing

The Micro Research Finland Oy (MRF) PMC Event Receiver Card (EVR) is used to receive global timing data and to provide hardware triggers for data acquisition.

Data Processing

The system uses embedded Linux with a real-time patch to provide deterministic processing. New software drivers were developed for the Struck digitizer and the new AFE. These new software components were integrated into the existing BPM application. Figure 4 shows the BPM software architecture.

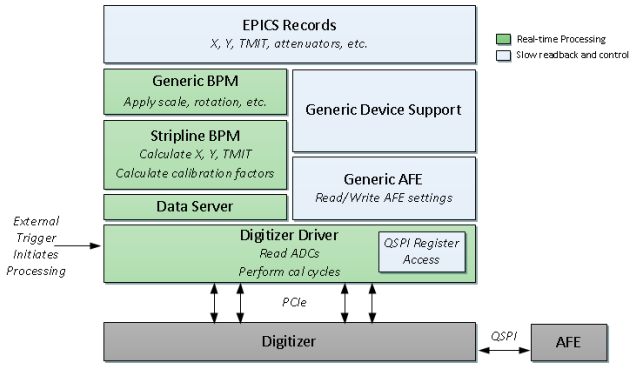

Figure 4: BPM software architecture.

The BPM data acquisition and processing is event-driven. At beam time, an external hardware trigger from the EVR initiates the beam data acquisition. Once this is complete, the software internally triggers a calibration cycle. To reduce overhead, a DMA engine is used to transfer data to the CPU. The software receives an interrupt when the transfer is complete. Figure 5 shows the process flow of two consecutive acquisition cycles.

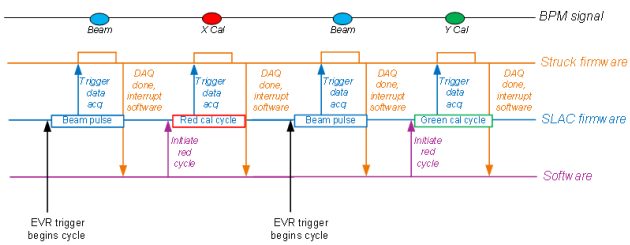

Figure 5: Data acquisition cycles.

The AFE firmware state machine executes the calibration routine and initiates digitizer data acquisition. The AFE has direct connections to the digitizer for real-time data acquisition handshaking. It also provides a QSPI interface to the digitizer for slow monitoring and control. Figure 6 shows the connections and data flow between the AFE and digitizer.

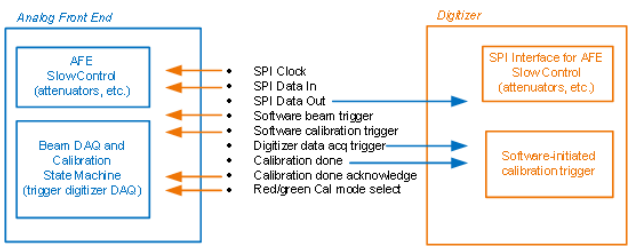

Figure 6: AFE-Digitizer interface.

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INITIAL RESULTS

Prototypes of this system have been tested in the LCLS Linac and at the PAL ITF [3].

Figures 7 and 8 show the measured beam position resolution of LCLS Linac BPMs, including the prototypes. The four red data points show the prototype data. The two points on the left are early prototypes; the two on the right are later prototypes with improved resolution.

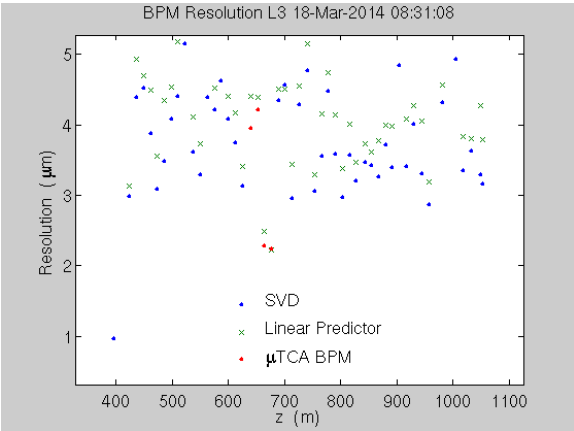

Figure 7: LCLS Linac BPMs measured beam position resolution at 160 pC bunch charge.

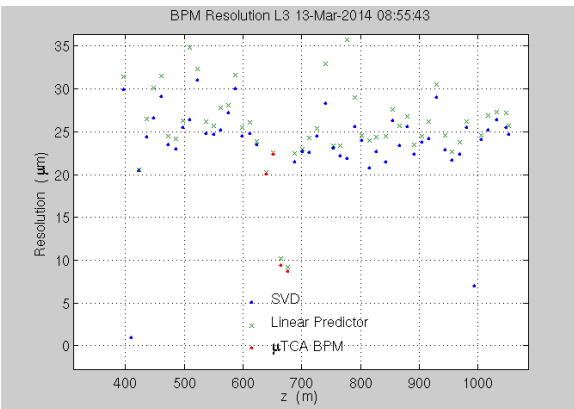

Figure 8: LCLS Linac BPMs measured beam position resolution at 20 pC bunch charge.

Figure 9 shows data taken at LCLS, plotting the position resolution as a function of bunch charge, from 20 pC to 150 pC. Within the dynamic range of the system, the position resolution should increase linearly as bunch charge decreases, until it reaches its resolution limit. Units BPM27201, BPM27301, BPM27401 are early system prototypes. The other two are legacy LCLS BPMs. The PRD limit shows the resolution requirement for the early prototype.

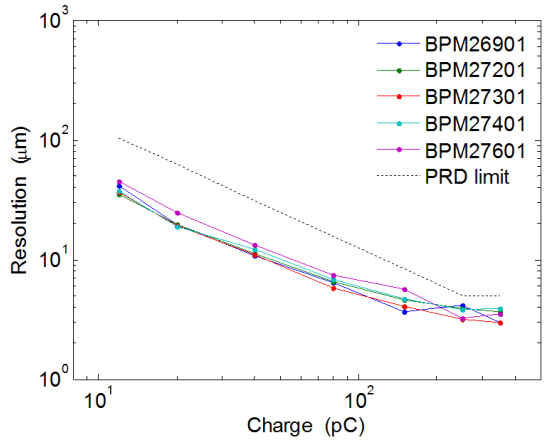

Figure 9: LCLS Linac BPMs dynamic range.

The BPMs at PAL ITF are on movers, which can be used to compare measured position as a function of actual position. The BPM system is expected to be linear within +/- 1 mm from the BPM center in the X and Y transverse planes. Figures 10 and 11 show X and Y data for a single BPM.

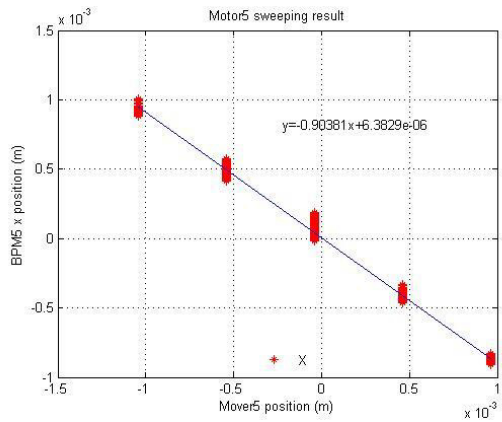

Figure 10: PAL ITF BPM measured versus actual X position.

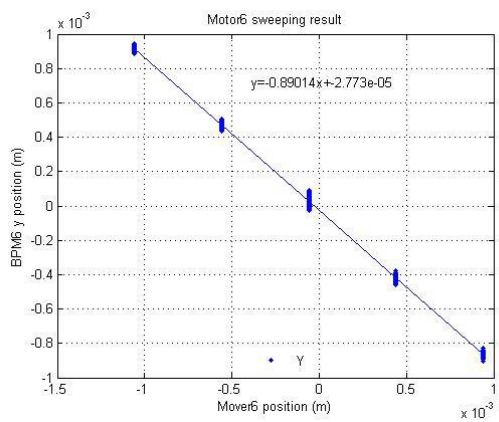

Figure 11: PAL ITF BPM measured versus actual Y position.

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FUTURE USE

The PAL XFEL facility will use this system for its 144 Stripline BPMs. This system will be commissioned with beam in early 2016.

SPEAR is currently using two of these BPMs in its transport line and plans to install more in early 2016.

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